Stability Analysis of Bus Architecture

9/14-15/2004

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Agenda

- Trend/Evolution of Distributed Power Architecture (DPA), and Type of Bus Architectures
- Stability Analysis of Bus Architecture
Trend/Evolution of DPA and Type of Bus Architecture
Trend of DPA (Distributed Power Architecture)

1970’s
- DPA level 1
  - Unit type DC-DC
  - 48Vin
  - 5V

1980’s
- Level 2
  - Card type
  - 5V

1990’s
- Level 3 (Isolated solution)
  - Board Mounted Type DC-DC (Brick Converter)
  - 3.3V
  - 1V

2000’s
- Level 4 (Bus Architecture)
  - Bus converter
  - 48Vin
  - AC

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2000’s
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  - 48Vin
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Non-isolated (POL)
Example(1)

Fully-regulated (Brick) +POL

Brick

3.3/5Vin POL

5V, 3.3Vbus

Front end/
Battery plant

48V

Capacitors

OPT/IF 3.3V

Memory 2.5V

1.8V-1.1V

ASIC/FPGA

Regulated Intermediate Bus (3.3V/5V)
Example(2):
Un-regulated bus converter + Wide input POL-

Front end
(Narrow input)

Bus converter

Wide input POL

48V

Un-regulated 12V, 9.6V

Opt/IF

3.3V

FPGA/ASIC

1.8V-1.2V

uP

1.5V-1.1V

Capacitors

Un-regulated 12V, 9.6V
Example (3):
Fully-regulated bus converter (Brick) + POL-

Brick

Narrow/Wide input POL

48V

Front end/
Battery plant

Regulated 12V

Capacitors

OPT/IF 3.3V

FPGA/
ASIC 1.8V-1.2V

uP 1.5V-1.1V
Variation of Bus Architecture
-Application point of view-

- Un-regulated bus
  - Server, Storage, Datacom
  - Narrow input (43-53Vin)

- Fully/Semi-regulated bus
  - Telecom normal input 36-60Vin

- Fully-regulated bus
  - ATCA (36-72Vin)
  - Telecom wide input 36-72Vin
Relation between Input Sources and Bus Converters, and Bus Voltages

### Input sources
- Narrow input (43-53Vin)
- Telecom normal input (36-60Vin)
- Telecom wide input, ATCA input (36-72Vin)

### Bus converters
- Un-regulated
- Semi-regulated
- Fully-regulated

### Bus voltages
- Un-regulated 12V
- Un-regulated 9.6V
- Semi-regulated 12V
- Semi-regulated 9.6V
- Fully-regulated 12V
- Fully-regulated 9.6V
- Fully-regulated 5V
- Fully-regulated 3.3V
POL Input Range of Bus Voltage

Bus Voltage

Vin (V)

12V fully-regu

Un-regu 4:1

Un-regu 5:1

5V fully-regu

3.3V fully-regu

12V wide input POL cover

3-5V input POL cover
Stability Analysis of Bus Architecture
Considerations

• Evolution of the bus architecture allows flexibility and low cost concept in different applications.
• Because of many different types of bus architecture, the stability of the system has become an important issue.
• This report discusses stability for 3 types of bus converter and POL based on impedance analysis. To simplify the comparison, we have ignored the impact from internal interference between bus converter and POL.
• The spec. used in this simulation of the power supply is 48Vin, bus voltage of 12V and POL of 1.5Vout/30Aout with 10 units in parallel. The detail value of the components such as output inductance, capacitance and cross-over frequency, etc are shown in table 1.
• The example of the simulation can not cover all phenomenon, but we could leverage this method to practical applications.
Concept of 3 types of Bus Architectures

- **Un-regulated Bus converter**
  - Input: 48V, 12V, 9.6V, 43-53V, 36-60V
  - Output: 48V, 12V, 9.6V

- **Semi-regulated Bus converter**
  - Input: 48V, 12V, 9.6V, 43-53V, 36-60V, 36-72V
  - Output: 48V, 12V, 9.6V
  - PWM Controller

- **Full-regulated Bus converter**
  - Input: 48V, 12V, 9.6V, 5V, 3.3V, 43-53V, 36-60V, 36-72V
  - Output: 48V, 12V, 9.6V
  - PWM Controller
Table 1

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vin</td>
<td>Input Voltage</td>
<td>48V</td>
</tr>
<tr>
<td>Vb</td>
<td>Bus Voltage</td>
<td>12V</td>
</tr>
<tr>
<td>fcb</td>
<td>Crossover frequency of Bus Converter</td>
<td>150-25kHz</td>
</tr>
<tr>
<td>Lb</td>
<td>Output Inductor of Bus Converter</td>
<td>0.5-10µH</td>
</tr>
<tr>
<td>Cb</td>
<td>Output Capacitor of Bus Converter</td>
<td>0.4-15mF</td>
</tr>
<tr>
<td>rlb</td>
<td>Resistance of Lb</td>
<td>10mΩ</td>
</tr>
<tr>
<td>rcb</td>
<td>ESR of Cb</td>
<td>5mΩ</td>
</tr>
<tr>
<td>Vo/Lo</td>
<td>Output Condition</td>
<td>1.5V/30A</td>
</tr>
<tr>
<td>fcp</td>
<td>Crossover frequency of POL</td>
<td>50kHz</td>
</tr>
<tr>
<td>Lo</td>
<td>Output inductor</td>
<td>1.5µH</td>
</tr>
<tr>
<td>Co</td>
<td>Output capacitor</td>
<td>1000µF</td>
</tr>
<tr>
<td>rl</td>
<td>Resistance of Lo</td>
<td>10mΩ</td>
</tr>
<tr>
<td>rc</td>
<td>ESR of Co</td>
<td>5mΩ</td>
</tr>
</tbody>
</table>
Output Impedance (Zo) of bus converter

Open loop

$$Z_o(s) = \frac{\Delta V_{bus}}{\Delta i_{bus}} = \frac{1}{P(s)} \left\{ s^2 L_b C_b r_c + s \left( L_b + C_b r_{Lb} r_{cb} \right) + r_{Lb} \right\}$$

(Un-regu, Semi-regu)

Where,

$$P(s) = s^2 L_b C_b + s C_b \left( r_{Lb} + r_{Cb} \right) + 1$$

Closed loop

$$Z_{o\_close}(s) = \frac{Z_o(s)}{1 + T(s)}$$

(Fully-regu)

Where, T(s) is a transfer function of Bus converter

$$T = H(s) \cdot G_c(s) \cdot PWM \cdot G_{dv_b}(s)$$

H(s): sense gain, Gc(s)=transfer function of the compensator, PWM: gain of the comparator, Gdv(s)=Vs/P(s) x (sCr_c+1)
Input Impedance (Zin) of POL

\[ Z_{in}(s) = \frac{1}{Z_N(s)} \cdot \frac{T(s)}{1+T(s)} + \frac{1}{Z_D(s)} \cdot \frac{1}{1+T(s)} \]

Where, \( T(s) \) is a transfer function of POL

10 modules in parallel
General Un-stability Phenomenon

Output impedance and input impedance

Frequency response of loop gain.
To get 12db margin, 10,000uF of capacitor is needed at bus.
Fully-regulated

Increase the cross over frequency of full-regulated bus converter damp the peak of Zo.

Further more, 2,000-3,000uF capacitor help To get 10deb margin.

Cb and Zo : fcp=15kHz (Full-regulated case)
Un-regulated bus converter has small output inductance such as 0.5μH, so it is stable without large extra capacitor at the bus.
Conclusion

• Semi-regulated bus converter + POL
  – Need a large bus capacitor compare to un-regu. and fully-regu. to be stable.
  – Can cover telecom normal input range (36-60Vin)
• Fully-regulated bus converter + POL
  – By adjusting a cross over frequency of bus converter, it can reduce the bus capacitor for stability rather than semi-regu.
  – Can cover telecom wide input range (36-72Vin)
• Un-regulated bus converter + POL
  – Most stable (means less capacitor than others).
  – Can cover limited input range (narrow range of 43-53V)
• In a practical application, the bus capacitor should be designed by “ripple”, “transient response”, “stability” consideration.
Product for Bus Architecture
Bus Converters

Un-regulated Bus converter (4:1)

iEB series: 12V/300W (Quarter brick size)

iQD series: 12V/150W (Eighth brick size)

Fully-regulated Bus Converter (Brick: 12V, 5V, 3.3V)

iEA series

iQB series

iQM series
POLs

12V wide input range (6-14V)

PMH series

Vo = 0.75-5V
Io = 16A

3-5.5V input

iAA series

Vo = 0.75-3.63V
Io = 15A

iBA series

Vo = 0.75-3.63V
Io = 8A