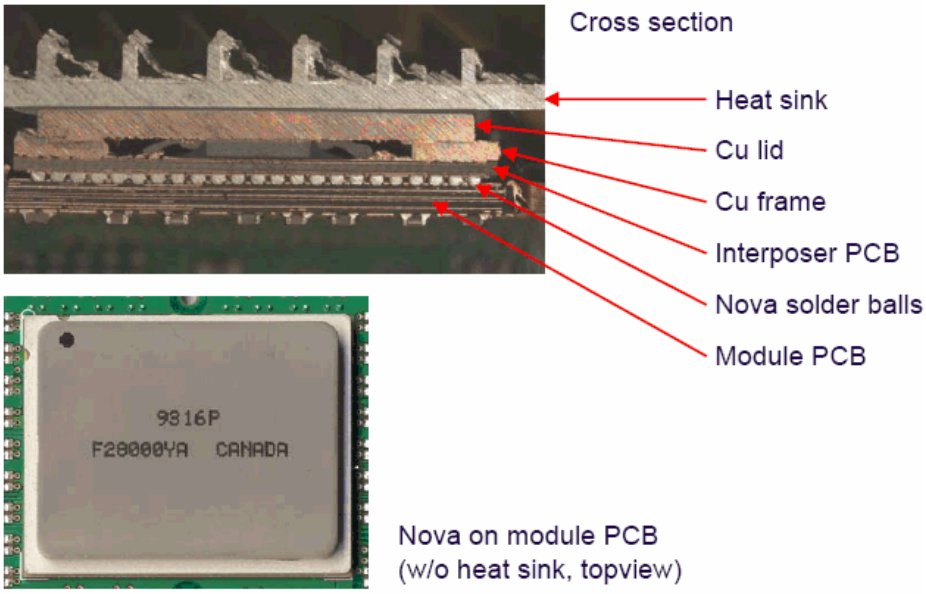
IBM PCB - OS Symposium



Faster, reliable and lower cost electronics through innovative technology integration

IBM
Bldg 400
Research Triangle Park, NC

June 19, 20 & 21, 2007

Day 1

Topic	Presenter	Time
Registration		08:00-08:30
Admin, logistic remarks	Ahmad Katnani	08:15-08:30
Session Chairperson	**Maurice Bland**	
Technology requirements		
Key note speaker	**Gregg McKnight, CTO IBM- STG**	08:30-09:00
X-series/ blades	Moises Cases, IBM	09:00-09:20
Enterprise System Overview	Harald Pross, IBM	09:20-09:40
Blue Gene & other systems	Todd Takken, IBM	09:40-10:00
Break		**10:00-10:30**
Session Chairperson	**Moises Cases**	
Technology roadmap		
PCB Technology Requirements	Bruce Chamberlin, IBM	10:30-10:50
OS Technology Requirement	Ed Blackshear, IBM	10:50-11:10
IPC Technology Roadmap	Dieter Bergman, IPC	11:10-11:40
Industry capability & gap data	Dave Wolf, CAT Inc	11:40-12:10
Lunch		**12:10-01:30**
Session Chairperson	**Don Thomas**	
Application challenges		
PCB challenges and Mfging solutions	George Dudnikov, Sanmina	01:30-02:00
Thin Core Challenge for Organic Substrates	Glen Thomas, Kyocera	02:00-02:30
PCB Memory/ IC simulation	Lei Shan, IBM	02:30-02:50
Substrate Design Challenges	Stefano Oggioni, IBM	02:50-03:10
Break		**03:10-03:40**
Chairperson & Moderator	**Martin Goetz**	
Packaging solutions: meeting the challenge & tradeoffs	Martin Goetz, IBM-STG	03:40-04:00
Panel discussion The purpose of this panel is to discuss the requirements and challenges, define potential solutions, identify risks and tradeoffs, examine the synergy and leverage areas between PCB & OS	IBM & Suppliers panelist	04:00-05:30
Poster		05:30 - 07:00
Adjourn & other activities		

Day 2

Topic	Presenter	Time
Session Chairperson	**Eddie Kobeda**	
Key note speaker	**Mark Morizio, Director IBM- ISC**	08:30-09:00
Material development		
Low D_k, D_f Materials for Substrates	Shigeo Nakamura, Ajinomoto	09:00-09:20
Difficulties in High Speed Low Loss Resin Systems	Terry Takata, MEW	09:20-09:40
A novel Halogen Free Material for Substrates	Tim Lee, Doosan	09:40-10:00
The Road to Pb-free-Compatible PCBs. The View from MSA Base Camp	Wayne Rothchild, IBM	10:00-10:30
Break		10:30-11:00
Chairperson	**Bruce Chamberlin**	
Design & Mfging challenges		
Design optimization of Blade Center	Pravin Patel, IBM	11:00-11:20
Design challenges with HDI	Justin Bandholz, IBM	11:20-11:40
Solid micro via plating	Marie Yu, Multek	11:40-12:00
Embedded caps; PCB, substrate applications	Erdem Matoglu, IBM	12:00-12:20
Laminate Substrates for IBM Chip Pkg., Current and future Requirements	David Russell, IBM	12:20-12:40
Lunch		**12:40-02:00**
Chairperson	**Pui-Shan Hou**	
Cost optimization		
Design for Supply Chain: System cost optimization	Bill Lohmeyer, IBM	02:00-02:30
PCB mfg & cost drivers	John Stephen, Merix	02:30-02:50
Reducing Costs with Supply Chain Modeling; *Case Study : Embedded Technology*	Chet Palesko, SavanSys Solutions LLC	02:50-03:10
ISC FCPBGA Laminate Design for Cost Initiative	Doug Powell, IBM	03:10-03:30
Break		03:30-04:00
Chairperson	**Roger Krabbenhoft**	
Electrical characterization Techniques		
Impact of moisture and temperature on D_k & D_f of substrate laminate materials	Jean Audet, IBM	04:00-04:20
Tighten Impedance tolerance & EBW technique for loss measurements	Brian Butler, IBC	04:20-04:40
Electrical characterization of PCB materials	Ege Engin, GaTech	04:40-05:10
Practical Considerations in the Modeling and Characterization of PCB Wiring for Multi-GHz Operation	Alina Deutsch, IBM	05:10-05:40
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Day 3

Topic	Presenter	Time
Chairperson	**Ed. Blackshear**	
Future Technology		
Key note speaker	**Stefano Oggioni, IBM- ISC**	08:30-08:50
Emerging electronics packaging technologies	Jon Aday, Amkor	08:50-09:20
Packaging Technology Development to Support New System Architectures	Claudius Feger, IBM	09:20-09:50
3D Chip Stacking Technology with low volume Lead-Free Interconnections	Katsuyuki Sakuma, IBM	09:50-10:10
Break		10:10-10:30
Chairperson	**Lei Shan**	
Approaches & Applications		
PCB Design and Fabrication Challenges for 20 Gb/s and Up	Voya Markovich, EI	10:30-11:00
Copper Metallization on Smooth Resin Plane for Fine Line Formation and High Signal Transmission Delivery	Syoichi Koyama, Shinko	11:00-11:20
Smooth copper foil for high speed applications	Takuya Yamamoto, Oak-Mitsui	11:20-11:40
Development of Advanced FCPBGA using Maskless Laser Direct Imaging Method	Seon-Ha Kang, Samsung Electro Mechanics	11:40-12:00
Developments in the Area of Dielectric Layers for Flip Chip Packages	Karl, Dietz, Dupont	12:00-12:20
Reliable glass fabric and ultra-thin glass fabric for HDI	Ysohsiharu Suzuki, Nittobo	12:20-12:40
Adjourn ... Have a safe trip home		

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Adjourn & other activities		

Key note speaker

Enterprise System Overview X-series/ blades Blue Gene & other systems

Jan Janick, IBM, VP Modular and Storage Development

Abstract:

Computing technology has evolved dramatically from the 20th century to the 21st century. This was a period of accelerating changes for the IT industry and all of its supporting technologies and industries, The IT industry has gone from isolated and complex computing system environments (glass rooms) to personal computing and mobile environments in a distributed fashion at a rapid rate through a world-wide network. This evolution has transformed the IT industry in many ways demanding lower cost, minimized complexity, and increased business efficiency. These needs created a battle for technology leadership driven by end-to-end system solutions requiring strong emphasis on cost, performance, reliability (up time), and innovation that matters to the customer.

In this presentation, a series of emerging system technologies, core products, and core technologies are briefly described in the context of the System x & Blade server development strategy. The design challenges, design drivers, and design implications are highlighted and some examples given as they relate to electronic packaging technologies.

Enterprise System Overview

Harald Pross, IBM- STG Enterprise Server

Abstract

Enterprise Systems develops Servers for pSeries, iSeries, zSeries and sSeries brand. Each Series has its own portfolio from Low End to High Performance. These systems are based on IBM proprietary processor architectures based on Power Architecture and zSeries Architecture. A brief overview of the Enterprise System Server Families will be presented. This presentation describes the i,p,z,sSeries server strategy, design drivers and the impact to electronic packaging technology. This drives to unique electronic packaging requirements from low cost to very high layer count, from densest processor package to largest printed circuit boards, from 1 EIA low end drawer to very high performance, high complex multi processor systems.

X-series/ blades

Moises Cases, IBM, Chief Engineer - System Technology for Modular and Blade Servers

Abstract:

System x and Blade servers designs are primarily driven by industry standards and vendor supplied component roadmaps. The primary drivers are lower cost, minimized complexity, end-to-end solutions, and increased business efficiency. This presentation describes the System x and Blade servers design strategy, design drivers, and design implications as they relate to electronic packaging technologies. In addition, a brief overview of System x and Blade server product roadmap is presented. Performance evaluations and roadmaps are presented for industry standards and their impact on PCB technology requirements and associated electrical design challenges such as dielectric material, back drilled vias, and I/O circuit complexity.

Package and PCB needs for IBM 2010 massively parallel systems

Todd takken, IBM- Yorktown Research Center

Abstract

Large, massively parallel systems BlueGene/Q and PERCS will be pushing the limits of affordable module and card technologies in the 2010 time frame. Chip sizes will have expanded beyond today's 18 mm x 18 mm maximum silicon size on an organic module, with chips in the 400 mm^2 to 550 mm^2 range, and packages handling increased current, faster signals, and more connections. High speed card-level signaling will progress to the 6 - 8 Gbit/sec range for short (under a foot) busses to memory, and 4 to 6 Gbit/sec for backplane nets approaching a meter in length through multiple connectors. The exact signaling speed will likely depend on the affordability of a low loss FR4 alternative. Backplanes will increase in size, and layer count. Thick cards and high signaling speeds will require stub control, possibly through multi-laminate card cross sections. In order to minimize IR loss as chip voltages fall and currents increase, the last stage of power conversion will move closer to the load, and intermediate voltage distributed in the rack will rise. Some fraction of the circuit cards will therefore need to distribute and isolate 350+ volts.

IBM PCB Technology Challenges and Roadmap

Bruce Chamberlin, IBM-ISC Procurement Engineering

Abstract

There are many technology drivers that define the printed circuit board technology requirements. This presentation describes the key technology drivers and how they define IBM printed circuit board technology. Breaking this down to specific PCB design attributes, such as line width, PCB thickness, and via pitch, the IBM PCB roadmap will be presented, with decreasing clarity the farther out we look. Challenges presented include IBM specific reliability requirements for qualification, manufacturing test, and restrictions to design.

IBM Organic Substrate Technology Requirement

Ed Blackshear, IBM- ISC Procurement Engineering

Abstract

IBM Future needs for organic substrate technology across the application spaces we serve, ASIC's, game processors, server processors will be described. Technology challenges will be identified, thermal, performance, wire-ability. Reliability issues in adapting organic substrates to an always on environment will be considered. The role of organic substrates in emerging applications will be discussed.

IPC Technology Roadmap

Dieter Bergamn, IPC

Abstract

This presentation would be on the newly released IPC 2006/2007 Technology Roadmap. This presentation would be an overview of the new roadmap, PCB technology, Packaging substrate Technology, and an Assembly Technology, with an emphasis on those topics that were new or upgraded for 2006/2007.

New topics for 2006/2007 include:

- Design models
- Flex technology
- Reliability protocols
- Factory environment
- Equipment roadmap and
- Optoelectronic assembly

Industry capability & gap data

David Wolf, CAT Inc.

Abstract

The scope of the presentation is a follows:

1. Document current and historical rigid board manufacturing capabilities from the IPC PCQR² Database;
2. Validate "current" technology roadmap data and expand on roadmap information to include additional attributes; and,
3. Focus on historical data to make future projections.

PCB challenges and Mfging solutions

George Dudnikov, Sanmina CTO

Abstract

Electronic packaging drivers continue to demand increasing wiring densities, smaller features and finer line widths on PCBs. High speed digital applications are driving not only higher frequency transmission but also a need for improvement in BER (bit error rates). Specialized markets such as Medical and Defense/Aerospace have additional requirements for reduced form factor and weight as well as improved signal integrity and high reliability. Customer and Industry roadmaps forecast ever increasing technology challenges but sometimes overlook important variables such as cost , design/ yield limitations and other logistics.

This paper will present current challenges leading PCB fabricators are facing with advanced technology printed circuit boards and modules. Current solutions for handling higher I/O components including finer line geometry and stacked microvias will be reviewed. RoHS and lead free assembly effects that typically are overlooked will be presented. The paper will also discuss current achievements in 10 Gbps plus data transmission including laminate material and via structure effects on signal attenuation and BER. The paper will highlight some novel and newly developed technologies in the area of high speed materials, embedded passives and HDI structures which we believe will be enablers for next generation PCBs and packaging applications.

Thin Core Challenge for Organic Substrates

Tomoyuki Yamada, Kyocera

Abstract

In recent years, the electronics Assembly industry has seen a rapid migration to Flip Chip substrates because of their ability to provide high density, miniaturized packaging when compared to traditional packaging methods. Thus the Flip Chip substrate is now being used in a myriad of end applications from cell phones, to digital cameras and even High End Servers. The Organic Substrate provides several advantages over its Ceramic alternative. These include improved electrical performance, a thinner profile, superior mechanical properties and lower overall cost. Still, there are tradeoffs that need to be considered and one of these is the inherent CTE mismatch between the Die, the Substrate and the Printed Circuit Board. Organic substrates typically consist of an inner core surrounded by buildup layers and then solder resist. In order to improve the loop inductance, which is required for high speed signals, the inner core thickness has been steadily decreasing. Traditionally, Organic Substrates used an 800-1000 μm thick core. However, in recent years there has been a lot of pressure to make product with a 600 μm or even a 400 μm core. Of course, while the overall Loop Inductance is indeed improved, one of the tradeoffs is the degradation of the substrate flatness or warpage. Thus the challenge is how to maintain a flat substrate while still meeting the industry demand for a product with a thinner core. It has been shown that design features as well as processing are all major contributors to the final substrate warpage found in today's products. In this paper, the design contributors for substrate warpage are analyzed and explained. An ideal substrate design for the ultra thin core needed for the future is also discussed.

PCB Memory/ IC simulation

Lei Shan, IBM Yorktown Research Center

Abstract

The demand for data throughput in high-performance computing systems continues to drive increases in both data-rate and channel density, and therefore sophisticated packaging design becomes critical to reducing I/O power and maintaining signal integrity. Together with the stress of demands for cost minimization, this leads to shrinking design margins that require precise analysis of the interactions and tradeoffs between different packaging options and equalization circuits required to compensate for channel impairments that result.

In this presentation, both frequency and time domain simulation and modeling techniques will be discussed and verified with measured data. Some key channel impairments were analyzed to provide design recommendations, including transmission lines, via transitions, sockets/connectors, signaling schemes, current return paths, and signal conditioning. The increase in data-rate is associated with additional transmission line losses due to skin effect and dielectric dissipation. Via transitions/stubs and sockets/connectors are the major sources of discontinuity/parasitic and channel cross-talk. Further, the choice of signaling schemes, differential vs. single-ended, needs to be determined in early design stage without sufficient supports of hardware validation. In addition, to test the requirement of signal conditioning, corresponding hardware was fabricated and measured to correlate channel configuration and equalization complexity.

Future substrate Design Challenges

Stefano Oggioni, IBM ISC Procurement Engineering

Abstract

Design of large substrates with very large semiconductor device, which are densely populated with several thousands of interconnect bumps, has become a highly complex and multidisciplinary effort.
Increased demand at user interface performance, always translates into a growing complexity of the packaging solutions needed to address higher currents transfer, as well as into signal integrity issues and circuits capable of supporting higher speed data rates. While ASICs applications were in the recent past the demanding applications this is no longer true in these days. Riding the wave of the booming game industry the microprocessors designs are now responsible of stretching the technology envelope. They are pushing toward unexplored limits, every hierarchical level of the packaging development.
To makes things even more challenging, these applications are also shifting into solutions requiring multiple dies being mounted on the same carrier.
Even if with the creation of new tools and design support techniques, the learning process of designing these sophisticated substrates proceeds with major improvements at every technology turn; multiple design optimisation cycles, especially through electrical simulation and wiring exercises, seems to be unavoidable prior of reaching an acceptable working solution.
It also becomes more and more clear that the larger effort of a successful design still lies in the preliminary and preparatory work. This goes from mechanical modelling to electrical simulations of both micro and macro details, of a package that still has to be designed.
In the presentation some future challenges and technical thoughts will be introduced according to the available outlook of future package requirements.

Panel discussion

The purpose of this panel is to discuss the requirements and challenges, define potential solutions, identify risks and tradeoffs, examine the synergy and leverage areas between PCB & OS.

Poster Session

Abstracts start on Page 50

Day 2

Topic	Presenter	Time
Session Chairperson	**Eddie Kobeda**	
Key note speaker	**Mark Morizio, Director IBM- ISC**	08:30-09:00
Material development		
Low D_k, D_f Materials for Substrates	Shigeo Nakamura, Ajinomoto	09:00-09:20
Difficulties in High Speed Low Loss Resin Systems	Terry Takata, MEW	09:20-09:40
A novel Halogen Free Material for Substrates	Tim Lee, Doosan	09:40-10:00
The Road to Pb-free-Compatible PCBs. The View from MSA Base Camp	Wayne Rothchild, IBM	10:00-10:30
Break		10:30-11:00
Chairperson	**Bruce Chamberlin**	
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Design optimization of Blade Center	Pravin Patel, IBM	11:00-11:20
Design challenges with HDI	Justin Bandholz, IBM	11:20-11:40
Solid micro via plating	Marie Yu, Multek	11:40-12:00
Embedded caps; PCB, substrate applications	Erdem Matoglu, IBM	12:00-12:20
Laminate Substrates for IBM Chip Pkg., Current and future Requirements	David Russell, IBM	12:20-12:40
Lunch		**12:40-02:00**
Chairperson	**Pui-Shan Hou**	
Cost optimization		
Design for Supply Chain: System cost optimization	Bill Lohmeyer, IBM	02:00-02:30
PCB mfg & cost drivers	John Stephen, Merix	02:30-02:50
Reducing Costs with Supply Chain Modeling; *Case Study : Embedded Technology*	Chet Palesko, SavanSys Solutions LLC	02:50-03:10
ISC FCPBGA Laminate Design for Cost Initiative	Doug Powell, IBM	03:10-03:30
Break		03:30-04:00
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Electrical characterization Techniques		
Impact of moisture and temperature on D_k & D_f of substrate laminate materials	Jean Audet, IBM	04:00-04:20
Tighten Impedance tolerance & EBW technique for loss measurements	Brian Butler, IBC	04:20-04:40
Electrical characterization of PCB materials	Ege Engin, GaTech	04:40-05:10
Practical Considerations in the Modeling and Characterization of PCB Wiring for Multi-GHz Operation	Alina Deutsch, IBM	05:10-05:40
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Key note speaker

Integrated Supply Chain: Procurement Engineering challenges

Mark Morizio, IBM- ISC Procurement Engineering

Abstract:

OEM faces multiple challenges achieving optimized End-to-End solution especially with increasing dependency on externally developed technology and availability of partially tested diverse solutions. A strong Procurement Engineering and well integrated Supply Chain is of critical importance to ensure overall optimization and assessments of risk and dependencies. The future holds higher system complexity requiring high speed and major power and thermal management, fragmented technology and solution development activities necessitating well integrated supply chain and understanding of tradeoffs and risks. The presentation will discuss the challenges facing Procurement Engineering to meet product requirement in a dynamic market place at low cost without sacrificing quality and reliability and on schedule.

Low Dk, Df Materials for Substrates

Shigeo Nakamura, Ajinomoto

Abstract

Along with an increasing speed of clock frequency of MPU, there is a significant demand for lowering dielectric constant (Dk) and dissipation factor (Df) as properties of insulating materials used for packaging substrates. Ajinomoto Build-up Films (ABF) are used for packaging substrates widely due to their features of good reliability, excellent processability and well-balanced properties.

Their materials are mainly composed of epoxy resins and phenol type hardeners, which can achieve high glass transition temperature (Tg) and good insulation reliability. However, this cross-linking system generates the hydroxyl group which increase Dk and Df.

One of the most successful strategies for improving the electrical performance of epoxy systems is to combine cyanate esters that react with each other as well as epoxy resins without generating polar hydroxyl group. Recently, we have developed ABF-GZ series by using these formulation techniques. GZ series have less Dk and Df than those of present GX series, and moreover, they can achieve high peel strength of plated copper with low profiles due to their high mechanical strength. GZ series mainly consist of 2 types; one has the feature of high peel strength with very smooth copper profile, and the other type shows high Young's modulus and very low coefficient of thermal expansion (CTE).

In this presentation, we'd like to introduce our recent developments (GZ series) and show general properties as well as their processability of buildup technologies.

Difficulties in High Speed Low Loss Resin Systems

Terry Takata, MEW

Abstract

A newly developed multilayer board material based on non-polarity structure PPE (polyphenylene-ether) has excellent dielectric properties (r=3.5, tan=0.002 (1GHz)) and is capable of reducing transmission losses. The low coefficient of thermal expansion (Z-CTE) in the direction of the thickness (45×10-6/) provides a good through-hole reliability of PWBs with many layers and large thickness. The high thermal degradation temperature can resist the higher reflow temperature adopted for lead-free solder.
The material is expected for use in high-end electronic equipment such as network equipment, large-scale computers, IC testers, etc. requiring high-speed information transmission and large-scale operations.

A novel halogen free material for packaging substrates

Tim Leose, Doan

Abstract

Though the actual enforcement of the RoHS directive began last year, the IC packaging industry has been prepared lead-free processes for several years. Besides lead, the halogen materials caught attention of substrate fabricators since two brominated compounds have been listed with lead. Substrates are specially influenced by this regulation due to the common use of tin-lead solder and halogen flame retardants. Even though widely used TBBA, a typical halogen flame retardant, is not on the list, many assemblers push for the elimination of halogen compounds along with lead material in the substrate. To meet these demands, a novel substrate material, DS-7409HG, has been developed. The special filler and nitrogen containing resin were used as flame retardant instead of brominated one. The resulting material has DMA Tg of 240C. In addition, its CTE in z axis is less than 25ppm, which is lower than 50% of that of conventional FR-4. It also shows an excellent thermal stability, withstanding longer than 30min at 288C. The other properties of this material, such as modulus, Td and electric properties will be presented.

The Road to Pb-free-Compatible PCBs. The View from MSA Base Camp

Wayne Rothschild, IBM- ISC Procurement Engineering

Abstract

The status of and general trends observed during the quest to qualify IBM's PCB suppliers to build PCBs that are compatible with higher-temperature soldering processes will be discussed, with special emphasis upon laminates.

Significant technical and cost challenges are steadily being overcome in the first phase of this quest – compatibility with mixed-solder assembly processes (245 ^{o}C target), which is a growing need for IBM as SAC-balled BGAs are slowly overtaking Sn/Pb-balled BGAs in the marketplace.

Far more significant technical challenges exist in the second phase of this quest – compatibility with fully lead-free soldering processes for cards with higher thermal mass (260^{o}C target). New guidelines are emerging, with reliance on certain older guidelines being misleading and potentially leading to disasters.

Design optimization of Blade Center

Pravin Patel, IBM-STG Blades Development

Abstract

This paper describes the electrical and thermal design challenges encountered during the definition, design and verification of a BladeCenter™ system configuration utilizing high speed serial signal interfaces. This system uses Gigabit Ethernet (GbE), Fiber Channel (FC) and Infiniband (IB) interfaces for interconnecting processor blades through high speed cross-bar switches with built-in redundancy capability. A comprehensive electrical design methodology including accurate and detailed modeling and simulation of the complete design space is required to achieve the speeds provided by these standard interfaces using low-cost printed circuit board material. This paper also describes the modeling techniques were used to make the choices and tradeoffs unique to the midplane product and illustrate a sample validation or correlation between the simulation prediction and the hardware prototype. The power and thermal design challenges are described. The cooling solution needed to accommodate the overall system thermal requirement for minimum and maximum configuration is also discussed.

Design challenges with HDI

Justin Bandholz, IBM-STG Blades Development

Abstract

High Density Interconnects include various construction techniques for blind and buried vias. This presentation will explore the reasons why HDI is necessary and the concerns when implementing HDI in designs. We will also show how HDI can be utilized to reduce layer count and improve SI on PCBs.

Solid micro via plating

Marie Yu, Multek

Abstract

Solid via plating design is increasing because of the advantages that could not be found in conventional HDI plating. Solid via could avoid void generation in solder joint of BGA during assembly and hence strengthen bond strength and mechanical reliability. As via size getting smaller or aspect ratio getting larger, it is more difficult to plate them conventionally with high reliability. Besides, circuitry density can be increased and board size can be minimized by stack via design. Hence, solid via plating is a low cost solution of ELIC (Every Layer Interconnect). In current market, there are different methods of solid via plating such as vertical, horizontal, DC plating, pulse plating, panel plating, pattern plating and etc. This paper is to describe solid via plating principle, solid via reliability and product design.

Embedded caps; PCB,substrate applications

Erdem Matoglu, IBM-STG Blades Development

Abstract

Embedded capacitors in PCB and substrate applications are promising improvements in high frequency electrical performance of the next generation systems.

For high frequency signaling, embedded planar PCB capacitance can be used effectively as bypass capacitance. With minimum distance to the return current discontinuity, low parasitic inductance and high resonance frequency, embedded PCB capacitance technology is a viable solution for high frequency return current problem at connector to PCB junctions, reference plane changes, and mechanical or thermal cutouts.

Conventional substrate decoupling is implemented with surface mount IDC (Inter-Digitated Capacitors). The resonance frequency, hence the effectiveness of any capacitor is not only dependent on the amount of charge storage capacity, but also the loop inductance of its connection to the circuitry. In an organic substrate, depending on the organization of the power distribution layers, the IDC capacitors can have a large inductance loop. The larger inductance loop decreases the effectiveness of the substrate decoupling.

In this presentation, electrical performance improvements with embedded decoupling capacitors in organic substrate and planar bypass capacitors in PCB are discussed. The loop inductance for substrate decoupling capacitors is reduced using embedded technology. Resulting electrical performance improvements are illustrated with simultaneous switching noise simulations. For the PCB application, on going activity for building a functional test system is summarized and methods for measuring the effectiveness of the test system are presented.

Organic Laminate Substrates for IBM Chip Packaging: Current and Future Requirements and Challenges

David Russell, IBM-ISC Procurement Engineering

Abstract

The advancement of chip technology necessitates the advancement of the organic flip chip plastic ball grid array (FCPBGA) and flip chip plastic land grid array (FCPLGA) substrates used to package them. Compared to a few years ago, and looking out into the future, the demands on the packaging technology is steadily increasing. Higher chip I/O counts result in increased wiring density and therefore increase substrate body size or layer count. Substrates require thinner cores to support an increasing PTH density using smaller diameter PTH's. Thinner cores and larger body sizes have higher warpage which presents a yield challenge to the substrate fabrication and a reliability challenge to the packaging, especially for chips with low K dielectric. The interrelationships between wiring density, fabrication yields, and package reliability dictates compromise at every step of the development and qualification path. This presentation will provide an overview of the state of the art in flip chip laminate technology at IBM as well as the future trends and technology needs. Factors such as laminate ground rules, materials, and reliability challenges and their interrelationships in the module will be discussed.

Design for Supply Chain: System cost oprtimization

Mark Ivanhof, IBM-ISC Program Management

Abstract

In an effort to improve profitability, IBM's System x Development, Supply Chain, and Finance teams embarked on a joint mission to expand its cost focus beyond component Bill-of-Material (BOM) cost and consider the entire end-to-end (E2E) supply chain when designing their hardware products. The resulting Design for Supply Chain (DfSC) effort is not only innovating product design thinking, but also improving supply chain flexibility, reducing product complexity, and netting bottom line savings.

Product complexity undoubtedly drives cost. One design decision on a hardware component level can produce a ripple effect across the supply chain, which includes a worldwide network of numerous vendors, customers, IT systems, inventory sites, etc. Core DfSC principles involve designing components for commonality, simplification, and manufacturing flexibility without compromising market needs. This requires an awareness of how the design of a particular product relates to overall supply chain complexity, from our vendors' vendors through our customers' customers. One of the functions of the DfSC team is to facilitate this knowledge across functions, while finding opportunities that drive E2E savings.

Making E2E decisions requires quantification of supply chain costs on a part number level, where in the past we focused solely on BOM cost. For example, designing common components between products may require a higher BOM cost, but at the same time drive E2E savings. The DfSC team has created both a set of tools to quantify these supply chain costs, and a process to analyze potential savings opportunities, even integrating DfSC into System x's development process. These tools have also been applied to supply chain decisions, such as component integration and product sourcing strategies.

PCB Manufacturing and Cost Drivers; A Comparison to US and Asia Manufacturing Costs

John Stephens, Merix

Abstract

This presentation will cover cost drivers and manufacturing challenges between the US, Hong Kong and China. The presentation will highlight material, labor, overhead and technology cost implications and their impacts in different regions of the world. Cost comparisons will be provided on various design structures and methods that can be utilized for cost optimization.

Reducing Costs with Supply Chain Modeling; *Case Study : Embedded Technology*

Chet Palesko, SavanSys Solutions LLC

Abstract

As a result of increasing cost pressure on companies in all parts of the electronic manufacturing supply chain, new approaches must be taken to reduce cost across the supply chain - not just in one place. The problem with cost reduction focused on one part of the supply chain is that the reduction is accomplished at the expense of profit. The total underlying production cost is not reduced. Instead, somebody's profit is reduced. However, through the use of complete supply chain modeling, real underlying production costs can be reduced through better design decisions and technology choices.

These improved design and technology decisions can only be accomplished if the designers clearly understand the cost and yield impacts when making tradeoffs. They must be able to clearly see the downstream effects of their choices. On the other hand, suppliers must be able to communicate upstream and effectively influence design and technology decisions to improve manufacturability. Supply chain modeling effectively provides this upstream and downstream communication, and results in lower production costs and higher yield products.

An excellent example of the benefits of supply chain modeling is evident with embedding technology. Embedding is a common technology for miniaturization, performance improvement, or both. In some cases, embedding also provides an overall product cost reduction. However, embedding on the wrong design or choosing the wrong technology can be a cost disaster. In this presentation, we discuss the size and cost trade-offs of embedding and give guidance to help you assess whether embedding is cost effective.

Miniaturization through embedding is accomplished by incorporating circuit functionality in the board as opposed to placing components on the board. While there are a number of different embedding technologies, they can all be divided into two major categories. "Embedded passives" is a term which usually refers to the fabrication of passive devices such as resistors, capacitors, or inductors as part of the overall board fabrication process. "Embedded actives", or more accurately "embedded discrete components", refers to placing discrete components (usually either discrete passives or bare die) in the board prior to final lamination.

ISC FCPBGA Laminate Design for Cost Initiative

Doug Powell, IBM-ISC Procurement Engineering

Abstract

Design for Cost (DfC) is a design for manufacturability methodology with cost as the ultimate metric. In this presentation we will discuss Integrated Supply Chain Laminate Engineering's DfC Initiative. The goal of DfC is to provide the information and tools necessary to enable laminate designers to design a minimum cost laminate substrate for a given application. The methodology is focused on building design metric vs. cost models based on supplier validated metric to cost and yield correlation.

We will review the DfC initiative, with particular focus on the supplier interfaces required for the initiative to succeed. Items covered will include:

1. DfC methodology
2. DfC team structure
3. Metrics in play
4. Supplier interaction proposals

Current status of implementation

Impact of moisture and temperature on D_k & D_f of substrate laminate materials

Jean Audit, IBM-ISC Procurement Engineering

Abstract

This paper discusses the effect of the moisture and temperature condition on very high speed link using FCPBGA packages. Those external factors are significant on the insertion loss and on the impedance of the traces which are important on signal integrity. The limitation of the material set used in FCPBGA (Gx-13) are shown for very high speed links by taking account those external factors. Special attention should be taken in the design ground rules phase and a good understanding of the tolerance is needed.

Tighten Impedance tolerance & EBW technique for loss measurements

Brian Butler, IBC

Abstract

Current manufacturing process technologies make it difficult to achieve 5% impedance tolerances on printed wiring board interconnects. PWB fabricators often must resort to sorting techniques or must invest significant engineering resources to tailor their process to achieve results for a particular product. These lead to higher costs and thus higher prices. This discussion addresses the challenges faced by industry to achieve better impedance control. As the manufacturing processes change, the production impedance measurement methodologies, as an integral part of those processes, must improve to support tighter process control, and ensure product specifications are being met.

A new low cost, simple and repeatable production test method for measuring signal loss of printed wiring board (PWB) interconnects is discussed. The method uses Time Domain Reflectometry (TDR) to measure the transition duration of a step pulse through the PWB interconnect and determine the loss. The loss is presented as an “Equivalent 3dB Bandwidth”. Signal components with frequencies higher than the Equivalent Bandwidth frequency will incur more than 3 dB of loss passing through the interconnect. The method presents the total interconnect loss and does not describe loss components individually (e.g., dielectric loss and skin effect loss, etc.). This talk describes the specific process of measurement, a metrology capability assessment, and study results demonstrating the method’s ability to use the loss measurements to differentiate among PWB materials and structures.

High-Frequency Extraction of Dielectric Constant and Loss Tangent Using the Rapid Plane Solver Method

A. Ege Engin, GaTech

Abstract

New dielectric materials are being used for reducing electromagnetic interference (EMI) and improving signal integrity (SI). Examples include using high dielectric constant materials for decoupling and thin dielectric for managing return currents. As the frequency of the signals being propagated through such materials increases, the frequency dependent material properties become very important. We present a method to extract the frequency-dependent dielectric constant and loss tangent of such materials using rectangular power/ground planes. We have also developed a rapid plane solver for fast extraction of material properties and a causal modeling methodology based on the vector fitting algorithm.

An accurate extraction of the material parameters can be achieved by fitting electromagnetic simulation data to measurement data. The general procedure for the extraction of the material parameters using an electromagnetic solver and measurements on a resonant structure such as a plane pair can be summarized as follows:

1. Measurement of the test structure using a vector network analyzer (VNA).
2. Initial guess for the frequency-dependent dielectric constant and loss tangent.
3. Simulation of the test structure using an electromagnetic (EM) solver.
4. Comparison of the measurement results with simulation data especially at resonant frequencies.
5. Going back to step 3 with a refined guess of the material properties until there is a sufficient match between measurement and simulation results.

As the fitting process requires a lot of iterations, the efficiency of the simulator becomes very important. We apply a rapid plane solver [1], which provides a very fast method for
simulation of such rectangular plane pairs.

After extracting the dielectric constant and loss tangent, a causal model representing the permittivity needs to be developed for modeling purposes. A Debye model can be generated using the vector fitting method [2]. We have applied the rapid plane solver method on new thin (down to 16um) and high-K materials (up to a dielectric constant of 30) as well as on well-known materials, such as FR4, for verification of the results.

References

[1] A. E. Engin, A. Tambawala, M. Swaminathan, S. Bhattacharya, P. Pramanik, and K. Yamazaki, “Dielectric constant and loss tangent characterization of thin high-K dielectrics using corner-to-corner plane probing,” in Proc. Electrical Performance of Electronic Packaging, Scottsdale, AZ, Oct. 2006, pp. 29–32.

[2] B. Gustavsen and A. Semlyen, “Rational approximation of frequency domain responses by vector fitting,” IEEE Trans. Power Delivery, vol. 14, no. 3, pp. 1052–1061, July 1999.

Practical Considerations in the Modeling and Characterization of PCB Wiring for Multi-GHz Operation

Alina Deutsch, IBM Yorktown Research Center

Abstract

The continued increase in data-rates transmitted on long printed-circuit board interconnects require increased modeling and characterization accuracy and bandwidth. Typical data transmission in digital applications involves a variable data pattern with very fast transitions and long spans of steady-state levels. This implies that both the models representing these lossy transmission lines and the measurements need to be broadband in nature, from DC to close to 50 GHz for systems delivered in the 2005-2010 time frame [1]. Many of the effects that could be ignored in the past at lower frequencies are gaining significance. The slower risetimes that were used were tolerant of less accuracy or even non-causal models. Suppliers provided single value dielectric and loss tangent information, TDR-based impedance, and maybe some limited attenuation data. Nowadays, for multi-gigahertz operation, each component in a critical path contributes to signal distortion and affects system performance. Due to the need for lower power densities while also operating at higher frequencies, smaller swing signals are being used. Noise sources and reflections are becoming larger detractors from signal integrity and consuming the entire noise budget. This is why the properties of each component in the critical path have to be modeled and characterized with greater accuracy and at higher frequencies.

Broadband complex permitivity extraction of card insulators obtained on representative multi-layer structures is required. Accurate accounting of the roughness of the metallization and its impact on the total interconnect loss has to be made. Causal transmission line models have to be generated for accurate system performance prediction. Newer insulator materials with lower loss, lead-free compatibility, and better thermal and mechanical properties are being developed. Evaluation of the merits of such materials needs to be made with much greater accuracy even in the manufacturing environment. This leads to a closer scrutiny and redesign of the production-level process monitoring coupons currently used. Measurement of impedance needs to be extended to include frequency-dependent interconnect losses and dielectric material properties. Designers need the material parameters in order to generate broadband, predictive, causal models for a wide range of configurations or applications. Traditional frequency-domain characterization techniques, used for simpler structures, have been unable to extract the material properties due to the very large interface discontinuities present in most cards or boards. New de-embedding techniques are being investigated.

A very simple time-domain technique based on short-pulse propagation [2] will be shown to be able to extract the complex permittivity for printed-circuit-board materials over the frequency range of 2 GHz to 40 GHz. Examples will be given of some of the changing requirements for both modeling and measurement of representative printed-circuit interconnect characteristics and their relevance for overall system performance, delivery, and cost will be explained.

References

[1] G. Katopis, “Signal Interconnect Trends and Challenges Inside the CEC”, http://www.ewh.ieee.org/soc/cpmt/tc12/

[2] A. Deutsch, T-M. Winkel, G. V. Kopcsay, C. W. Surovic, B. J. Rubin, G. A. Katopis, B. J. Chamberlin, R. S. Krabbenhoft, “Extraction of $e_r(f)$ and tan$d(f)$ for Printed Circuit Board Insulators up to 30 GHz Using the Short-Pulse Propagation Technique”, IEEE Trans. Advanced Packaging, vol. 28, no. 1, Page 4-12, Feb. 2005.

Day 3

Topic	Presenter	Time
Chairperson	**Ed. Blackshear**	
Future Technology		
Key note speaker	**Stefano Oggioni, IBM- ISC**	08:30-08:50
Emerging electronics packaging technologies	Jon Aday, Amkor Claudius Feger, IBM	08:50-09:20 09:20-09:50
Packaging Technology Development to Support New System Architectures 3D Chip Stacking Technology with low volume Lead-Free Interconnections	K. Sakuma, IBM	09:50-10:10
Break		10:10-10:30
Chairperson	**Lei Shan**	
Approaches & Applications		
PCB Design and Fabrication Challenges for 20 Gb/s and Up	Voya Markovich, EI	10:30-11:00
Copper Metallization on Smooth Resin Plane for Fine Line Formation and High Signal Transmission Delivery	Syoichi Koyama, Shinko	11:00-11:20
Smooth copper foil for high speed applications	Takuya Yamamoto, Oak-Mitsui	11:20-11:40
Development of Advanced FCPBGA using Maskless Laser Direct Imaging Method	Seon-Ha Kang, Samsung Electro Mechanics	11:40-12:00
Developments in the Area of Dielectric Layers for Flip Chip Packages	Karl, Dietz, Dupont	12:00-12:20
Reliable glass fabric and ultra-thin glass fabric for HDI	Ysohsiharu Suzuki, Nittobo	12:20-12:40
Adjourn ... Have a safe trip home		

Key note speaker

Coming transitions in IBM substrates

Stefano Oggioni , IBM- ISC Procurement Engineering

Abstract:

There are many significant near term technology challenges for flip chip substrates. They include lead free solder implementation and fine pitch C4, both of which drive new pre-solder process technology development. Much Larger Silicon die qualifications. Increasing signal count and wiring density, with the resulting perforation leading to warpage issues. Implementation of low K dielectric in Silicon which, when combined with increased die size drives a need for low expansion materials.

Manufacturing challenges include the trend towards higher build up layer counts, increasing build cycle times where shortened cycle time is required. Substrates have become the long lead time item in product development. Introduction of next generation standard materials, including the selection process.

There is a need for shortened qualification cycle time, requiring the combination of substrate level and module level stress in substrate development. It will require close cooperation between substrate fabricators and customers to accomplish.

Emerging electronics packaging technologies

Jon Aday, Amkor Technology

Abstract

There is a dependent relationship between advances in substrate technology and packaging technology. Currently there are several new packaging technologies which are demanding a density increase in substrates for both small form factor packages and the very high end server type application space. The primary new substrate technologies include coreless or ultra thin core, chip embedded substrates, embedded capacitors, and very fine pitch substrates. These substrate technologies are required to enable the very high speed application space and high density package requirements, but new packaging technologies are also required to enable the silicon at the new target speeds and voltages as well. The new packaging technologies being investigated include copper pillar bump technologies, through silicon vias, overmolded flip chip packages, and many configurations of stacked die packages. This presentation will focus on the different packaging options which will require or enable new and unique substrate technologies.

Packaging Technology Development to Support New System Architectures

Steve Buchwalter, IBM Yorktown Research Center

Abstract

Increases in CMOS performance are becoming more challenging with every technology generation, and new packaging technologies will be needed for further improvements in system performance. This talk will describe approaches to address these challenges in areas such as three-dimensional integration, optical interconnects, and direct liquid cooling. The common theme is that packaging must not only continue to support CMOS interconnect, power, and reliability requirements but also facilitate new system architectures.

3D Chip Stacking Technology with low volume Lead-Free Interconnections

K Sakuma, Japan Research Center

Abstract

As the demand for higher wiring connectivity and shorter distance between chips has increased, so has the development of 3D packaging structures and system-on-silicon LSIs. [1-2] Of the existing 3D package technology options, wire-bonding remains the most popular method for low density connections of less than 200 I/O per chip. In the near future, however, it will become difficult to meet the increasing frequency and demand for wiring connectivity merely by increasing the number of the peripheral wire-bonds. In order to overcome such wiring connectivity issues, three-dimensional (3D) chip stacking technology using through-silicon vias is attractive because it offers a possibility of solving serious interconnection problems while offering integrated function for higher performance.

Some of the key technologies needed to enable chip stacking include silicon through vias and high-density lead-free interconnects. differnt interconnect metallurgy such as Cu/Ni/In, Cu/In and Cu/Sn were considered and the bonding conditions to optimize the bonding parameters were determined. The effect of intermetallic compound (IMC) formation on the mechanical properties of the joins is discussed. Unlike standard 100-micron C4 solder balls, very small solder volumes (< 6 microns high) were investigated. The mechanical properties were evaluated by shear and impact shock testing, while scanning electron microscopy (SEM) and optical microscopy were used to study the morphology of the IMC layers in solder joins before and after annealing. It was found that Cu/Ni/In and Cu/In interconnections have slightly lower shear strength per bump. While these values were lower than the Cu/Sn joins, the Cu/Ni/In chips passed the impact shock test for a simulated heat sink mass of $27g/cm^2$. The reasons for the differences in reliability of these metallurgies are discussed.

3D chip stacking using two-layers of chips with fine-pitch lead-free interconnects was demonstrated. The resistance of link chains comprising through-vias, lead-free interconnects and Cu links were measured using a 4-point probing method. The average resistance of the through-via including the lead-free interconnect was 21 mW.

PCB Design and Fabrication Challenges for 20 Gb/s and Up

Voya Markovich, EI

Abstract

The demand for high-performance and high speed in computing applications is challenging the conventional PCB design and fabrication methods.. Electronic packaging is evolving to meet the demands of higher functionality and higher speed. To accomplish this, new packaging needs to be able to integrate more dies with greater function, higher I/O counts, smaller pitches, and greater heat densities, while being pushed into smaller and smaller footprints. Traditionally, greater wiring densities are achieved by reducing the dimensions of vias, lines, and spaces, increasing the number of wiring layers, and utilizing blind and buried vias. However, each of these approaches possesses inherent limitations, for example those related to drilling and plating of high aspect ratio vias, reduced conductance of narrow circuit lines, and increased cost of fabrication related to additional wiring layers. As a result, the microelectronics industry is moving toward alternative, innovative approaches as solutions for squeezing more function into smaller packages. Assembly and packaging are bridging the gap by enabling economic use of the third dimension (3D packaging). System level integration is emerging. These approaches include System-in-Package (SiP), stacked die, or package stacking solutions. In addition to the trend toward miniaturization, new materials and structures are required to keep pace with more demanding packaging performance requirements. High speed packages, for example, as required for server and telecom applications, require low loss materials, better shielding, elimination of via stubs, and optical interconnection, both chip-to-chip and between packaging components This paper discusses a number of novel methods for extending packaging performance beyond the limits imposed by traditional approaches. One strategy allows for metal-to-metal z-axis electrical interconnection of subcomposites during lamination to form a composite structure. Conductive joints are formed during lamination using an electrically conductive adhesive (ECA). As a result, one is able to fabricate structures with vertically-terminated vias of arbitrary depth. Replacement of conventional plated through holes (PTHs) with vertically-terminated vias opens up additional wiring channels on layers above and below these vertical interconnections, and eliminates via stubs which cause reflective signal loss. Vertically terminated vias facilitate a more space-efficient package redesign. In addition, parallel lamination of testable subcomposites offers yield improvement, shorter cycle times, and ease of incorporating features conducive to high speed data rates. The requirements for signal speeds exceeding 20 Gb/s also drive a number of materials and processing challenges. Dielectric materials with very low loss are required and these materials should have either homogeneously dispersed reinforcing material or none at all. Copper conductors should be either very low profile or absolutely smooth if other methods of assuring adhesion are found. Semiconductor packaging will be placed as close together as possible on the PCB surface to minimize signal path length and there will be no space left for discrete components thus driving the need for embedded components. And all of these materials must be Pb free and compatible with Pb free assembly temperatures.

Study on Copper Metallization on Smooth Resin Plane for Fine Line Formation and High Signal Transmission Delivery

Syoichi Koyama, Shinko Electronic Industries Co. LTD

Abstract

Electroless Cu plating deposition has been generally used as metallization method onto dielectric resin plane as a semi-additive process for Cu trace formation for organic packages. In this method, to gain a high peel strength between the Cu trace deposited and the resin plane an anchor effect has been introduced. But the anchor structure causes some types of failures such as Cu seeding residues between lines which are from 5um to 10um below the plane. This is due to a number of deep dents scattering onto the resin plane closely that then retain Cu residues in the seeding layer removal process. These Cu residues are a source that can induce electrical short failures. However, over an over aggressive seeding removal process causes Cu trace detachment. Furthermore, a Cu trace with a rough morphology declines signal transmission delivery. Therefore, an alternative Cu metallization method needs to be developed.

In this poster new metallization methods such as graft copolymerization as well as micro or nano anchor affects are discussed. In the graft copolymerization method a peel strength of up to 0.7kg/cm was obtained on a smooth resin plane less than 0.1um in Ra. The Nano anchor structure with a primer achieved 0.8kg/cm. The signal transmission loss values were clarified by calculations and experiments demonstrated with Cu patterns on the smooth resin plane. An apparent difference was observed in transmission losses between the smooth and rough resin planes.

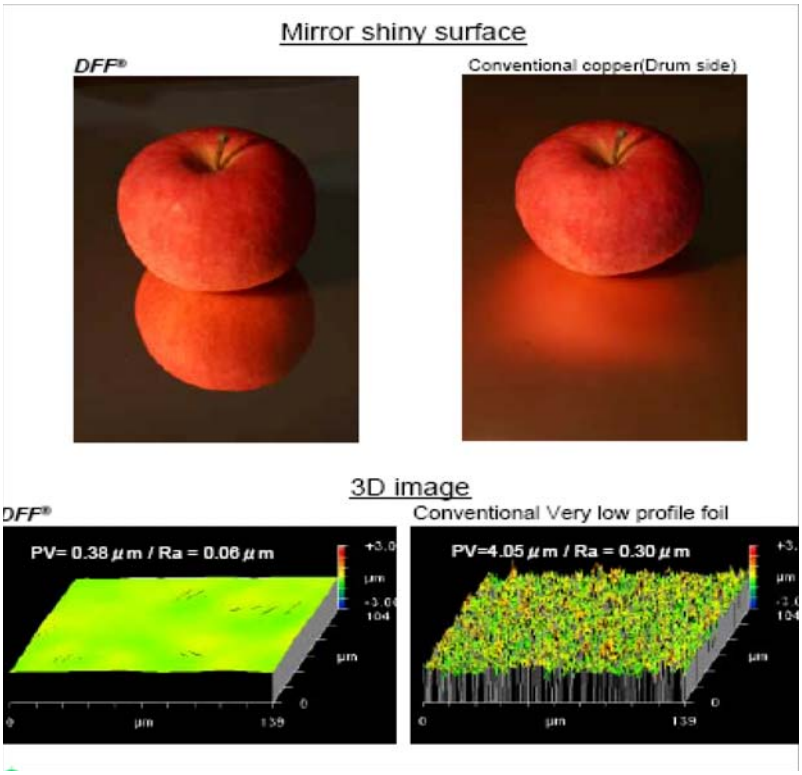
New Copper Foils for High Speed Systems and Their Performance Characteristics

John Andresakis, Oak-Mitsui Inc.

Abstract

During the last symposium we discussed the many factors that effect the propagation of signals through printed circuit boards. Among these concerns were the dielectric constant and loss tangent of the dielectric material as well as the bulk conductivity of the copper trace. It has been demonstrated that as the frequencies get higher, the phenomenon know as "skin effect" becomes a factor, as most of the signal now "travels" along the outside of the conductor.

Copper foils used in making printed circuit boards usually have the surfaces modified to enhance peel strength and to passivate the highly reactive surface of the copper. This mechanical and chemical modification of the surface can cause signal loss at high frequencies due to an increase in signal path (i.e. navigating the rougher surface) and increased resistivity (due to less conductive alloys on the surface). New copper foils have been developed to address the effects of copper profile and chemical modifications on the loss of signal attenuation at high frequencies. We will show both mechanical (such as adhesion to various resin systems) and electrical performance of these new foils. In addition these foils allow the manufacturing of extremely
tight lines and spaces.



Development of Advanced FCPBGA using Maskless Laser Direct Imaging Method

Young-Doo Jeon, Samsung Electro Mechanics

Abstract

As a demand for Flip-Chip packaging is increasing, FCBGA substrate is also widely accepted and developed in various application fields. Especially, in high-end applications, high routing density and fine registration are also required in the substrate. Lithography process using glass mask is conventional method to make routing patterns on photo-resist film. However, for specific applications which need small quantity and a lot of design revision, lithography process using glass mask will not be appropriate due to too much cost and time waste in preparation of glass masks. In addition, variation of panel dimension might cause poor registration capabilities due to fixed scale of glass mask.

The candidates for flexible lithography as well as dense routing capability is laser direct imaging (LDI) method. LDI method enables low processing cost without glass mask and flexible scaling control against dimensional change.

In this paper, feasibility and capability of LDI method was evaluated. With the largest panel size, 510x610mm^2, fine routing width/space of 18/18um and alignment accuracy of Max 15um could be achieved. The essential point in LDI process is development and optimization of photo-resist film called dry film. Depending on properties of the dry film, LDI capability is affected significantly. Consequently, a test vehicle with 42.5x42.5mm^2, 10 layer structure (4-2-4), 20/20um trace width/space and Max. 20um registration was manufactured using LDI method. Robust reliability of the test vehicle was convinced by following reliability tests such as temperature cycling test, biased HAST, and high temperature storage test.

Developments in the Area of Dielectric Layers for Flip Chip Packages

Karl Dietz, DuPont Electronic Technology

Abstract

Dielectric films for microvia build-up multilayers (BUM) for flip chip packages have enabled very high interconnect densities through semi-additive plating (SAP) of redistribution circuitry. Future microprocessor packaging requirements impose very demanding material property requirements and processing conditions on BUM materials. Work to achieve low CTE (coefficient of thermal expansion), low surface micro-roughness, acceptable copper adhesion and good flow properties is described. The need for very fine circuit lines and spaces may require an innovative solution like DuPont's Digital Circuitization (DC) technology which does not have the limitations of the SAP process but may introduce new challenges.

Reliable glass fabric and ultra-thin glass fabric for HDI

Ysohsiharu Suzuki, Nittobo

Abstract

The rapid developments of IT equipment are placing increased demands on printed wiring boards (HDI PWBs) in terms of high efficiency, high-density and lightweight. Industry experience has proven that glass fiber base materials are essential for highly reliable PWBs, in particular to obtain such characteristics as heat resistance, dimensional stability, mechanical strength and insulation reliability.

1. Reliable glass fabric

The laminate for HDI consists of glass fabric, resin matrix and copper foil.

Since the glass fabric dominates 35-45 volume % roughly, the quality of the glass fabric is related to the properties and reliability of laminates.

Nittobo improved the quality of glass fabric mainly by three following points;

a. Using high quality yarn material produced by Nittobo
b. b. Appropriate chemical finish for glass fabric
c. Spread out process for glass fabric

2. Ultra-thin fabric

Resin coated copper foil (RCC) is used widely as layer material for build-up (sequential) processing technology as a solution to these accuracy issues. However, in RCC's increasing use, much higher reliability such as no warp and crack and correspondingly improved dimensional stability is being demanded. We developed ultra-thin glass fabric to overcome these deficiencies of RCC. The ultra-thin glass fabric for microvias is able to bring high reliability and good processing and also used for very thin PWB and IC substrates package applications.

Poster 1

Dielectric Properties Extraction using Short Pulse Propagation

Eddie Tang, Senior Engineer, Group Technology, Elec & Eltek

Abstract

The performance improvement in high-end computers not only relies on the increase in the computing power of the processing unit, but also relies on the increase in data transfer rate. As printed circuit boards (PCBs) are used to electrically connect electronic components, they play a very important role in data transfer. PCB traces are surround by layers of dielectric, this dielectric medium interacts with the electric field of the electrical signal propagating through the traces and affects the signal integrity. Dielectric constant (Dk) and dissipation factor (Df) are the dielectric properties which are two of the origins of the signal loss in PCB. Dk determines the impedance and the propagation velocity while Df determines the loss assigned to the dielectric. Unfortunately, both Dk and Df are frequency dependent and the high-speed data consist of a wide range of high frequency components. When different frequency components experience different losses and delays, signal attenuation and distortion will be result. Therefore, an accurate dielectric properties extraction across a wide frequency range is essential for high-speed PCB development. The primary focus of this talk will be on the Short Pulse Propagation (SPP) technique that is developed by IBM. SPP is a powerful solution to extract the electrical parameters of a transmission line and the surrounding dielectric across a wide frequency range from 0 to 50 GHz, these parameters include resistance, capacitance, inductance, conductance, Dk, Df, etc. In this talk, SPP will be introduced and its functions will be discussed from the angle of a PCB manufacturer. E&E' experience on SPP will be shared and other current techniques of Dk and Df extraction will be discussed as reference.

Poster 2a

Integration of Embedded Capacitors into Flip-Chip Substrate Structures for Improved Power System Noise Decoupling and Charge Supply to the IC.

Daniel Amey, DuPont Electronic Technologies

Abstract:

The integration of embedded Thick Film capacitors and polyimide based planar capacitor laminate materials in IC packages has been investigated by a joint program sponsored by DuPont with the Georgia Institute of Technology Packaging Research Center (PRC). The PRC provided fabrication, electrical modeling and simulation and DuPont provided the component materials. Test vehicles with different designs were fabricated and tested. The test vehicles included embedded ceramic-fired-on-foil Thick Film capacitors with microvia interconnects and structures with planar capacitor laminate layers. Build-up dielectric layers were interconnected by semi-additive processing and laser microvia technology. Measured electrical performance data were used to create models of alternative package designs and to perform simulations to determine the designs offering the most effective power delivery and noise decoupling in accordance with substrate feature needs projected by the ITRS roadmap. The presentation will include integration of capacitors into substrate layers in close proximity to the IC, capacitor interconnections designed for low inductance and low impedance and achieving low target impedance over a mid-frequency range through capacitor designs and arrays resulting in a range of different resonance frequencies.

Poster 2b

All-Polyimide flexible laminates for high-performance applications

Thomas Fisher, DuPont Electronic Technology

Abstract

All polyimide, adhesiveless copper-clad flexible laminates have been used for many years in applications where consistent electrical and mechanical properties over wide temperature extremes and high reliability are required. All polyimide laminates are available in tight tolerance, uniform thickness up to 6 mils providing the design versatility needed for controlled impedance applications. In addition to outstanding environmental performance the material has excellent high frequency properties exhibiting a low dielectric constant (3.4) and low loss tangent (0.003), uniform and stable to 18 GHz and beyond.

Recent application of the material for flexible impedance controlled direct chip-to-chip interconnects has been reported to improve the bandwidth and interconnection lengths by two to three times over that of interconnects in an FR-4 printed wiring board. In comparative testing, raw bandwidth of about 9GHz in FR-4 was increased to 30 GHz using an all polyimide construction. Based on the testing performed the data shows the potential for the flex circuit approach to support up to about two times the data rate of FR-4. This presentation will describe the all polyimide material system, reliability testing and typical high frequency and high data rate applications of the material.

Poster 3

New Resin Developments for Electrical Laminates in Lead Free Solder Applications and Beyond

Bob Hearn, The Dow Chemical Company

Abstract

The regulation requiring lead-free solders for printed circuit boards (PCBs) has presented a number of challenges to our industry at virtually every stage of the process. For the brominated epoxy resins used to make a large fraction of the laminates that serve as the starting material for PCBs, the requirement for higher thermal stability has led to increased use of phenolic and other curing agents in place of dicy. The good news is that brominated formulations are available that can be used to make laminates that meet and exceed the highest IPC specifications for glass transition temperature (Tg > 170 °C) and decomposition temperature (Td > 340 °C). However, non-dicy curing agents lead to some compromises in other properties, especially toughness and copper adhesion. A general comparison of the properties of non-dicy vs dicy cure will be made, along with some guidelines for application.

The thermal stability of non-brominated resins is inherently greater than that of brominated resins, and meeting the highest Td specifications is not a challenge, even with dicy cure. Therefore non-brominated resins are well suited for lead free applications. Furthermore, unfilled non-brominated resins have improved dielectric properties and lower densities. However, non-halogenated resins are more expensive and exhibit greater water absorption. Achieving high Tgs (> 170 °C) can be a challenge, but this is now possible with commercially available materials. A comparison between brominated and non-brominated resins will be made.

Finally, a projection of the future laminate property requirements will be made along with the resin development efforts required to get there. made.

Poster 4

Characterization of Low Loss Materials for Lead-Fee Assembly

Jeng-I Chen, Derek Chang, *ITEQ Corporation*

Abstract

One of the major concerns for the implementation of lead-free soldering is the higher melting points of lead-free solders compared to that of the conventional Sn/Pb alloy. As a result, a higher peak reflow temperature is required during assembly processes. The increase in the processing temperature also leads to a significant impact on the reliability of printed circuit boards (PCB). In this paper, both bromine-containing low loss and halogen-free low loss PCB materials were studied for the compatibility with lead-free assembly. These materials showed low Dk/Df properties, suitable for high speed applications. These base materials were characterized for their thermal properties, such as Tg (glass transition temperature), Td (decomposition temperature), T-288 (time-to-delamination at 288), and CTE (coefficient of thermal expansion). In addition, PCB test coupons were prepared based on these low loss materials. Several reliability tests, such as interconnect stress test, thermal cycling, and insulation resistance, were performed on these coupons after different reflow preconditions. The impact of reflow process to the material performance is also discussed.

Poster 5

Dynamic Mechanical Analysis of Laminates

Joseph P. Kuczynski, IBM- STG

Abstract

Printed circuit boards must meet stringent requirements imposed by the elevated temperature processes required for mixed-solder assembly and lead-free soldering. In an effort to meet these requirements, laminate manufacturers offer a variety of resin materials ranging from high-temperature epoxies, polyphenylene ether/epoxy blends, polyphenylene oxide/triallylisocyanurate blends, cyanate ester/ epoxy blends, etc.[1-3]. Moreover, various curing agents, fillers, resin-to-glass coupling agents, glass reinforcement styles,, and toughening agents are typically incorporated into the resin to impart specific properties. Both the coefficient of thermal expansion (CTE) and the glass transition temperature (Tg) are two physical properties that have received considerable attention with respect to design of high-temperature laminates [4-5]. It is well known that CTE mismatch between the copper and the laminate within a PCB results in stress upon the copper that may manifest itself as opens within vias, at the interfaces between internal lands and plated-through hole barrels, as well as open traces. Since the CTE of resin materials below the Tg is typically is on the order of 5X lower than the CTE above Tg, a typical laminate design strategy is to produce a resin that exhibits a high Tg without adversely impacting other properties. Numerous factors affect the ultimate Tg of the resin, including the functionality of the monomer(s), crosslink density, the cure profile, and absorbed moisture. Within the electronics industry, Tg is determined via differential scanning calorimetry (DSC) as per IPC-TM-650 [6]. However, due to the multilayer construction of current circuit boards coupled with sample size limitations, DSC has been shown to be an inadequate technique for measurement of the glass transition temperature. The endotherm in the DSC is often ill defined, of marginal quality, and may be convoluted with stress relaxation and/or volatile outgassing at elevated temperature. Dynamic mechanical analysis (DMA) has been demonstrated to provide far greater information relative to not only the Tg, but also physical property depression due to moisture plasticization and incomplete resin conversion in various high-Tg laminate systems. Several case studies regarding a phenolic-cured epoxy resin and a cyanate ester/epoxy blend will be discussed.

Poster 6

Laminate Development and Applications

Louis Lin, Nan Ya

Abstract

1. Low Dk materials.

Normal FR4 material cannot meet the requirement of high-speed circuit design. In order to reduce dielectric constant value from 4.6 to 3.8, NAN YA is developing new resin system to combine with low Dk glass cloth. Our goal is to develop low cost and low Dk materials for high frequency applications.

2. **The challenges of higher temperature Lead Free process**

An Introduction to Laminates with Higher Heat Resistance and Reliability Temperatures of lead-free solder are 20 ~ 30 higher than those of traditional tin-lead solder. In addition, the lead free solder is less adhesive to tin, most assembly houses may consider to raise the temperature in solder to improve manufacturability and improve the throughput. Higher operating temperature and longer cycle present serious impacts to the heat-resistance for traditional FR4 material. The conventional wisdom of high Tg being equivalent to high heat-resistance is no longer valid in a lead free era. Instead, characteristics such as the temperature of decomposition (Td), time to deleamination by TMA (T-260/T-288), and coefficient of thermal expansion (CTE), etc., are major indices referenced by the PCB industry in choosing the high heat-resistance laminate materials. Among them PN-cured laminate materials are the most favorable, mainly because the resin of PN-cured laminate materials have more aromatic structure, which has relatively lower water absorption and better heat resistance: Td > 350 ,T-288 > 15min,and CTE value on total expansion <4%. In addition, considering from the point of cost, it can also be improved based on dicy-cured FR4 to make its price and manufacturability close to those of currently used standard FR4.

Poster 7

Design and routing for high speed application using HDI PCB

Richard Tu, Compeq

Abstract

The poster will cover the following topics:

1. Stack-up structure of digital systems using HDI PCB (eg. [PTH + L1-2-3 + L1-2] or [PTH + L1-3 + L1-2])
2. Design and routing benefits of HDI PCB (eg. routing density, layout flexibility, SI benefits)
3. Introduction to HDI process
4. Impedance control for HDI process (eg. material for build-up layer, build-up dielectric layer thickness control, plating thickness and line width control)
5. Progress in HDI technology (eg. HDI application in cellular phone, notebook, sever or rigid flex)

Poster 8

A New Probing Technique for High-Speed/High-Density Printed Circuit Boards

Kenneth Parker, Agilent Technologies

Abstract

Bullock, in 1987 [Bull87] provided design-for-test (DFT) rules for probing printed circuit boards for In-Circuit testing. Many of these rules stand in good stead even today. However, recent technical advances in operational board speed are leading some to believe that In-Circuit testing cannot be performed on the high-speed sectors of boards soon to be designed. Due to the increasing usage of high-speed circuitry, there is worry in our industry that In-Circuit testing will be marginalized with no good substitute available. It is the purpose of this paper to show how access can be maintained, even on highly dense gigabit logic boards.

Poster 9

Reduction of Discrete Capacitors and EMI using Embedded Capacitance layers: Comparison of Simulated versus Actual Results.

John Andresakis, Oak-MItsui Technologies

Abstract

Reduction of chip capacitors on the PCB surface using a Power/Ground simulation tool was compared with actual results. We found good correlation of the simulated to actual performance. Furthermore we observed the effect that thin capacitor substrates have as power/ground planes. The voltages were more stable with greatly reduced resonances. Reduction of these resonances results in lower EMI from these PCBs. We will show that by using thin core planes and this simulation tool one can reduce the number of discrete capacitors and get better electrical performance.

Embedded Capacitor technology has been driven by the need to save board area and/or reduce board size, increase functionality, lower costs and improve electrical performance. Many examples exist for the use of this technology (current capacitive material is used in the high end computing industry , mostly for telecom and networking applications). For these particular high end PWB applications, embedded capacitor technology has been utilized to enhance signal integrity, reduce impedance at high frequency and dampen noise, and not necessarily to remove discrete capacitors.

A number of papers have been published regarding development of materials for embedded capacitors and the advantages of incorporating embedded capacitors in PCBs. There are not, however, many details as to the number of discrete capacitors that can be removed by utilizing this technology.

As other applications are being looked at for incorporating embedded capacitors (such as the modules used in cell phones and laptop PCs) the ability to predict the number of discrete components that can be removed is critical to the decision to use the technology.

In this presentation, we will compare the electrical performance results of simulation of boards with and without embedded capacitors. The number of discrete components the model predicts we can actually remove to actual boards will also be compared. We will also show two examples of reduction of EMI due to the use of thin layers. With a good predictive model, the decision to utilize embedded capacitors is simplified.

Poster 10

Thermal Analysis Tools : Developing Materials with Superior Thermal Oxidative Stability for Lead Free Soldering Conditions

Roger Tietze, Huntsman Advanced Materials

Abstract

The Printed Wiring Board Industry today has a bewildering array of materials to choose from for Printed Circuit Board applications. There are many requirements such as non-halogen, low loss, high Tg°C, and these are just a few of the properties that are needed for most board designs. However; one of the newest and most demanding requirements today is the need for Printed Circuit Board substrate materials that can withstand the extremely high temperatures of the lead free soldering process. This paper will discuss a varied range of thermal analysis techniques that currently are in use and are relative to our industry. We will describe the data concept of each of these analysis techniques so they might be used to determine which materials are particularly suitable for use with lead free soldering conditions in Printed Circuit Board production environments.

Poster 11

System In Package (SiP) and Stacked Package Solutions

Denis Soldo, Ansoft Corporation & Wayne Nunn, NXP Semiconductor

Abstract

Faster switching, higher pin count, lower supply voltages, and the need for greater density are placing new demands on signal and power integrity. While BGA and flip-chip package solutions are already widely deployed, next generation designs are targeting System in Package (SiP), stacked package solutions, and System on Chip (SOC) to meet future demanding performance goals. This paper discusses the challenges with advanced package design and highlights a new approach to design and verify performance of the package, board, and circuit together. Novel stacked package designs called Package on Package (PoP) is discussed with application for differential, high-performance interfaces like DDRx, PCI Express, SATA. The paper shows how to incorporate critical layout effects from the IC and package to evaluate system performance. By harnessing the power of today' compute power combined with clever data management, this paper shows how to solve very large packaging problems accurately and efficiently. The many advantages, including the ability to rapidly analyze various routing alternatives, is shown throughout the work. Post route verification for full designs using 3D EM tools is highlighted.

Poster 12

New efficient monitoring method of impedance

Jean Audet, IBM_ ISC Procurement Engineering

Abstract

This paper discusses a new efficient monitoring method for impedance control using statistical impedance distribution generated from physical dimension data which are collected from manufactured products. In the method, statistical analysis is conducted on physical dimensions using randomly generated simulation data based on manufacturers' data, as well as measured data to predict potential impedance tolerance in a manufacturer's capability; this is used to "tune" the design accordingly.

Poster 13

Advancement in flying probe test for PCB

Jeff Hagopian, Microceaft

Abstract

MicroCraft is a manufacturer of high end flying probe test equipment for the printed circuit board industry. With over 1,300 systems installed world-wide, MicroCraft is on the forefront of the next technology wave. The employment of Latent Defect Testing, to detect near faults and verify the signal integrity of critical nets has seen a re-birth and MicroCraft has been an integral part of its resurgence. The ability to detect mouse bites, dish downs, cracked lines and more, has truly broadened the scope of detectable defects.

This presentation will highlight the increasing demands on electrical test equipment to keep pace with decreasing lines and spaces. High accuracy flying probe testers, HYBRID grid/prober systems, and novel testing advancements will allow tomorrow's test departments to conduct more tests with less tools. Continuity, Isolation, Embedded Resistor, Embedded Capacitor testing are all conducted in one, single pass. Systems with minimum pad accuracy of 15 um are becoming a reality.

As HDI technology becomes more complex, so too must the test equipment and methods which verify the product's integrity.

Poster 14

Via Reliability – A Holistic Process Approach

David L. Wolf, Conductor Analysis Technologies, Inc.

Abstract:
New materials and processes are being developed and introduced to the printed circuit board industry with the objective of ensuring the reliability of via interconnects under the harsh conditions required for lead-free assembly. In order to validate the "goodness" of these materials and processes, reliability studies must be performed. However, these studies are often based upon a small number of samples and the samples may or may not have been produced with the same set of manufacturing processes intended for the production product. Furthermore, the samples must be produced from a controlled and capable process in order for the reliability results to be valid.
The IPC PCQR^2 Database provides a holistic approach to understanding the capability, quality and reliability of production printed circuit board processes. This presentation will summarize recent findings of the impact of lead-free assembly on via reliability and provide case studies documenting the need for controlled, capable and uniform printed circuit board manufacturing processes.

Poster 15

Design Rules to Prevent Damage in Telecom/Server Printed Circuit Boards Subjected to Pb-Free Reflow

Craig Hillman, DfR Solutions, LLC

Abstract

The use of lead-free solder requires higher reflow temperatures, which can potentially damage printed circuit boards (PCBs.) High density PCBs are especially susceptible to thermal damage resulting from elevated reflow temperatures, which can exceed 250˚C. This study will develop design rules to prevent damage in PCBs subjected to Pb-free reflow. The test coupons consist of 26 layers, and each circuit contains 40 daisy-chained plated through holes. The first phase of this research involves simulated reflow of two board designs until changes in resistance and capacitance are measured, or until cracking or delaminating of the boards is observed. Two sets of boards, each containing samples of both designs, will be repeatedly reflowed with peak temperatures of 245˚C and 260˚C. The second phase of the study involves characterizing the effects of moisture absorption in the laminate material, ITEQ-IT180. Boards at 0%, 25%, 50%, and 100% moisture saturation will be cycled through reflow using the same test parameters and failure criteria as those described in phase 1. The performance of the boards in phases 1 and 2 will be compared to evaluate whether moisture absorption accelerates failure mechanisms such as delaminating in PCBs.

Map


IBM; TRun right before the gate
Raleigh-Durham Airport
Northern Wake Expy
Commerce Blvd
International Dr
Aviation Pky
Lumley Rd
National Guard Dr
Airport Exit
Terminal Blvd
Globe Rd
Briar Creek Pky
World Trade Blvd
Page Rd
Airport Rd
Nelson Rd
Slater Rd
Chin Page Rd
Silicon Dr
Old Page Rd
Emperor Blvd
Hops Rd
Chapel Hill Rd
Morrisville
Cornwallis Rd
Laboratory Dr
Davis Dr
E Institute Dr
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Sorties Ct
540
40
54
147
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Your feed back is essential for continuous improvement. Please take a moment to answer the following questions:

Quality Measurement Survey	**Response: 5- Most positive 1- Most negative**				
Question	**5**	**4**	**3**	**2**	**1**
Were you satisfied with the communication and clarity of objectives?					
Please comment below any suggested improvement in communication.					
Was the lead time sufficient?					
How do you rate the facility?					
How do you rate the location?					
Please comment below if a different location would have better served the meeting.					
How do you rate the agenda (topics and					
allocated time)?					
How do you rate the panel discussion?					
Please comment below on the weaknesses and strengths of this approach.					
Overall, how do you rate the quality of presentations?					
Has the Symposium met your expectations?					
Would you attend this Symposium again?					
At what frequency, circle one 6 12 18 24 months					
What is the factor that contributed to your answer above?					
What are the weak points that we could eliminate for future Symposiums?					
What are the success factors that we should build on?					
What do you like to see in future Symposium?					
Overall comments/ suggestions					