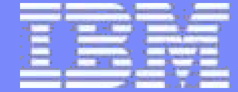

Lead-Free HASL: Balancing Benefits and Risks for IBM Server and Storage Hardware

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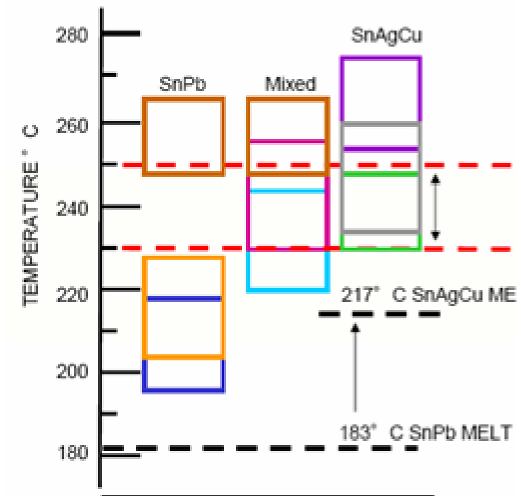
Agenda

- High Reliability, High Complexity Lead-Free Assembly Challenges
- Technology and Supply Chain Strategy
- Scope, Intent, Objectives
- Approach
- Horizontal vs. Vertical HASL Processing
- Quality & Reliability Assessment
- Test Performance to Date
- Summary
- Questions

Electronic Card Assembly & Test Point of View

High Reliability LF Challenges

- Process windows are much smaller for lead-free PCBAs
  - Applies to primary attach and rework processes
  - As thermal mass & complexity ↑, process windows ↓
  - Significant challenges remain for large server backplane assemblies
- Process window issues affected by surface finish selection:
  - PCB raw card shelf life
  - SMT pad wetting performance
  - Time between SMT reflow and PTH wave soldering control
  - PTH barrel fill performance
  - ICT electrical contacts / NDF minimization



- Surface finish integration into high reliability designs requires assessment of:
  - Characterization of process window expansion benefits and yield performance
  - Ensuring PCB laminate reliability is not degraded due to HASL process
  - Thermo mechanical reliability performance; using high reliability test protocols
  - Understanding of actual application environments of product

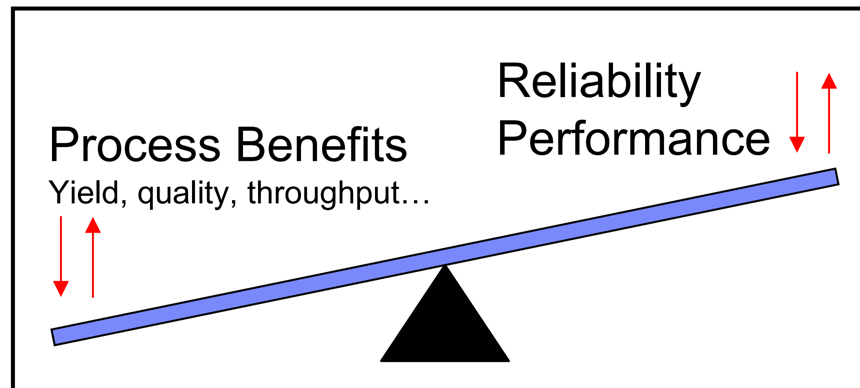
- Surface finish selection must therefore balance the following elements:
  - Process window expansion benefits
  - Longer term hardware reliability performance
  - Representative environment operating conditions

- Surface finish selection can help with these elements
  - Each option has its own benefits and drawbacks; all must be evaluated

	Benefits	Drawbacks / Risks
OSP HT	**Proven reliability** Harsh environment performance High incoming quality	**Small process windows** Handling and storage PTH hole fill issues **Test pin probability**
Immersion Silver	Similar thermal fatigue reliability to OSP Improved pad wetting and PTH barrel fill	Incoming quality control **Harsh environment corrosion risks**
Lead-Free HASL	**Test pin probability** Improved pad wetting and PTH barrel fill **Larger process windows reported** **Corrosion resistance improvements**	**Potential PCB damage HASL process** **Unknown high reliability performance** Minimal industry data Supply quality concerns

- Overall Technology Strategy
  - Realize lead-free process window expansion without compromising PCB and second level assembly reliability performance
  - Perform numerous deep dive evaluations to improve technical understanding of LF HASL
- Supply Chain Strategy
  - If lead-free HASL process shown to be technically feasible → work with PCB and CM suppliers to continue qualifying, specifying, controlling, and integrating finish as option
  - Identify any switching costs and adoption issues associated with potential conversion

Challenge: Balancing Output Performance



Inputs: Design, Assembly Materials, PCB Materials, Interconnect Technologies, Supply Sources, Cost

Strategic Approach for HASL Assessment / Potential Integration

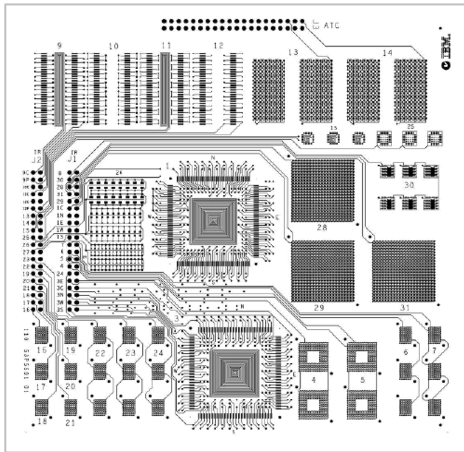
Phase	Focus of Study	Core Activities
Phase 1	Fundamentals / Feasibility Studies	General Quality Levels PCB Reliability Risks Cumulative Heat Exposures Horizontal vs. Vertical Process
Phase 2	Advanced Environmental Studies	SIR, Corrosion Resistance Ionics, Cleanliness
Phase 3	Yield / Quality Improvement Monitoring	Volume Assessment Multiple PCB Suppliers Multiple Card Designs
Phase 4	Supply Chain Support / Implementation	Manufacturing Readiness Equipment / Capital Supplier Qualifications
Phase 5	PCB Supplier Qualification Process Modifications	BAU Process Changes Quality Monitoring / Metrics

- Scope
  - Potential option for all IBM xipzServer brands, tape & DASD Storage brands
  - Potential LF HASL implementation not intended as a replacement to OSP
  - Alternate lead-free alloy HASL evaluation → not SnAgCu based alloys
- Intent
  - Determine if lead-free HASL can be used in IBM server / storage designs
  - Technical feasibility studies uncovering benefits and risks with LF HASL
  - If Phase I and II acceptable, then conduct additional phases

- Phase 1: Fundamentals / Feasibility Study Objectives

1. Assess general quality level of applied HASL finish; uncover general PCB reliability risks associated with lead-free HASL surface finish
2. Understand PCB construction reliability risks during multiple HASL rework exposures at PCB fabricator (1X through 4X) and through assembly processing
3. Examine differences between PCB quality after (a) HASL application versus (b) assembly process simulation exposures
4. Assess comparison of general quality of applied HASL finish and thermal exposure to the PCB of (i) horizontal vs. (ii) vertical HASL processing methods

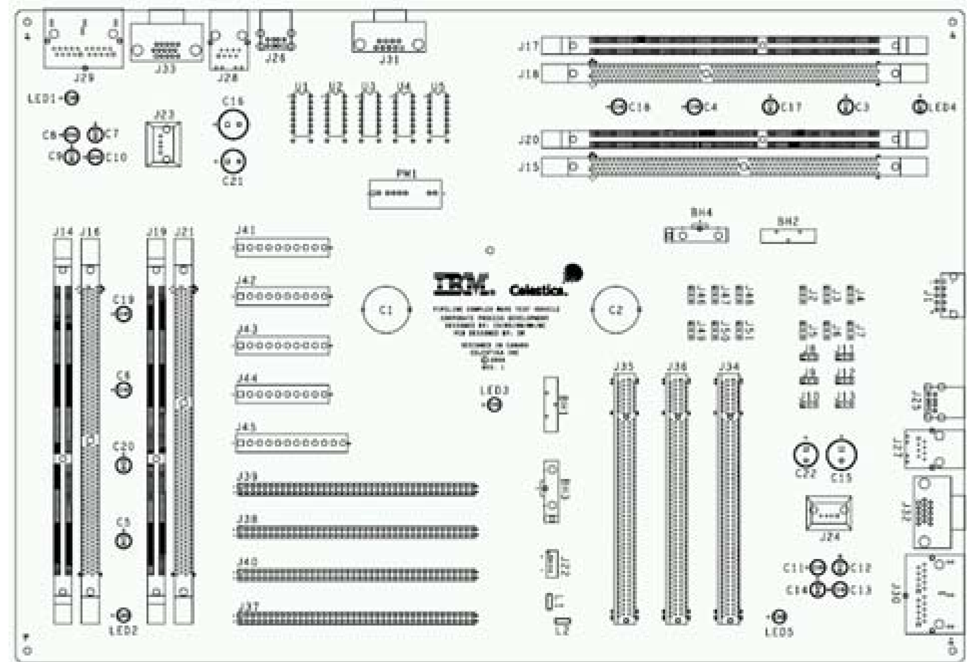
- Evaluation Hardware / Designs



IBM SIR Test Vehicle

Focus: Surface Insulation Resistance

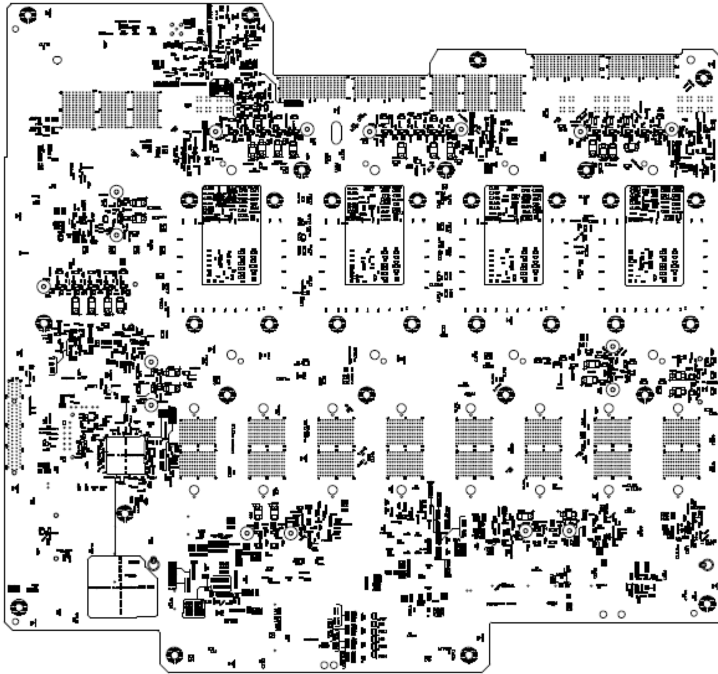
- Surface Finish: Lead-Free HASL
- All assembly materials applied
- **50C/80RH; 15V DC bias; 300 hrs**
- Maintain resistance above 10 MΩ
- Coupon size: 12mm^2; 0.094”



Engineering Test Vehicle

Focus: PTH barrel surface finish quality

- Multiple HASL rework evaluations (1X through 4X)
- **Multiple connector families found on IBM product**
- Time zero and assembly simulation PCB evaluation
- Horizontal HASL processing
- 11 x 16”; 0.120”; 22 layers; 10 2oz grounds; 14oz Cu



IBM Product Vehicle 1

Focus: SMT Pad Flatness / Quality
- Vertical vs. Horizontal comparisons
- **SMT pad flatness assessment**
- Tooling hole clearance
- 10 x 16”; 0.096”; 16 layers; 1 &2oz Cu

IBM Product Vehicle 2

Focus: ECAT Qualification Test Suite Performance
- Fully functional qualification assembly hardware
- **Reliability performance using IBM Server high-reliability stress testing protocol**
    - ATC 0-100C, 1CPH; HTS 125C, 1000 hrs
    - Combination shock & vibration
    - 4pt bend testing and construction analysis

- **IBM Collaborative Working Group**
  - Lead-Free alloy suppliers
  - PCB suppliers
  - Contract manufacturing suppliers
  - HASL equipment manufacturers

- Lead Free Hot Air Solder Level (HASL)
  - SnCuNi (SN100CL)
  - SnAgCu(X) (SACX) follow-on studies in progress
- PCB Laminates
  - IBM qualified and suitable for Lead-Free assembly (245C ratings)
  - 4 different laminates used within study to date; various designs
- HASL Process Deep Dive
  - Vertical vs. Horizontal Processing Comparison
  - **Target:** link PCB and surface finish defects to actual HASL process steps

- Evaluation Testing
  - Laminate Integrity After PCB Fabrication
    - Time zero quality, specifications, thickness control
    - Long term laminate reliability performance
  - Laminate Integrity After Electronic Card Assembly
    - Cumulative raw card performance after assembly & rework simulation
    - Product vehicle qualification performance
  - 2nd Level Assembly Qualification Stress Testing (Operation Simulation)
    - Mechanical fragility via shock & vibration
    - Thermal fatigue resistance (ATC and HTS)

    Plus, combination thermomechanical testing
  - Harsh Environment Corrosion Resistance via SIR

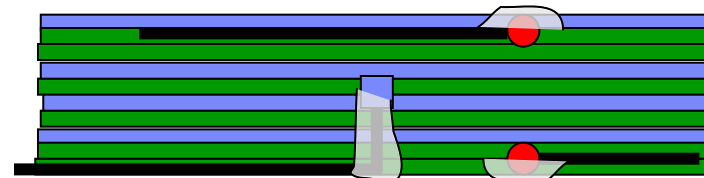
Assembly & Rework Heat Exposures → Thermal Stress Heat Exposures → Atmospheric Exposures

Horizontal vs. Vertical Processing

- **Intent:** Characterize the SN100CL HASL surface finish process, by monitoring peak temperatures and times during vertical and horizontal HASL processes
- **Status:** process review completed single tool supplier; 2nd supplier under eval

- IBM 1st to thermally profile LF HASL processes; significant findings
  - Profiled both vertical and horizontal HASL processes (much like SMT reflow)
  - Multiple TCs used to monitor actual PCB temperatures at surface and core

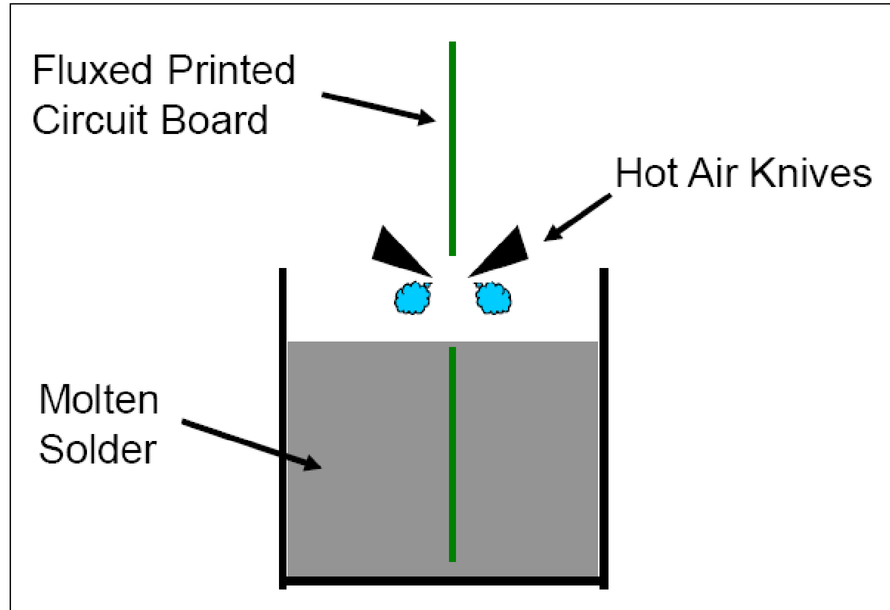
- Vertical HASL Tooling
  - Small footprint on shop floor
  - Capital cost range $50-$100K USD
  - 95%+ of all PCB fabricators in use



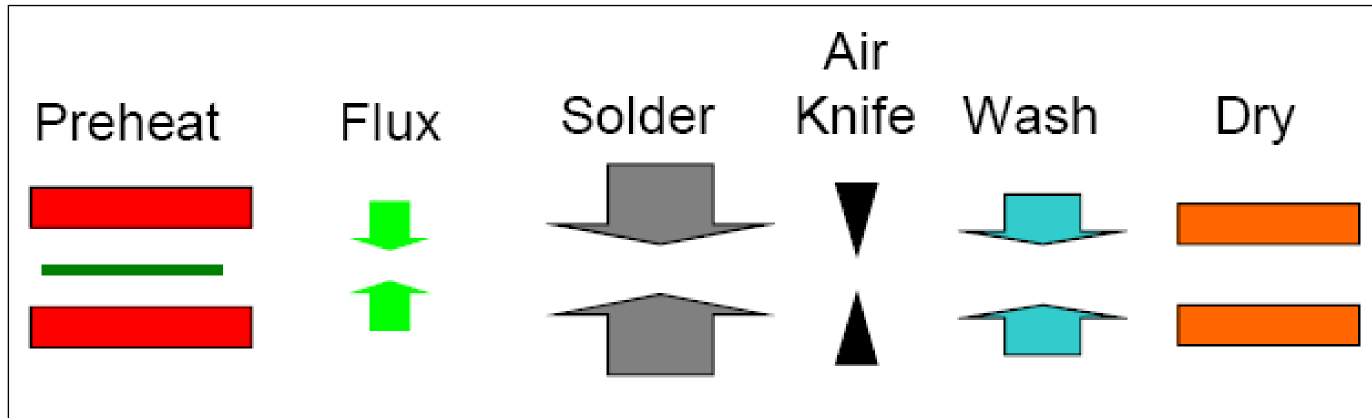
Surface and Core Temperatures

- Horizontal HASL Tooling
  - SMT like footprint on shop floor
  - Capital cost range $500-$850K USD; significant switching costs

Horizontal vs. Vertical Processing

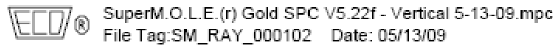


Vertical: First in, last out



Horizontal: First in, first out

Vertical Profiling Example

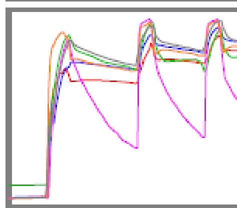


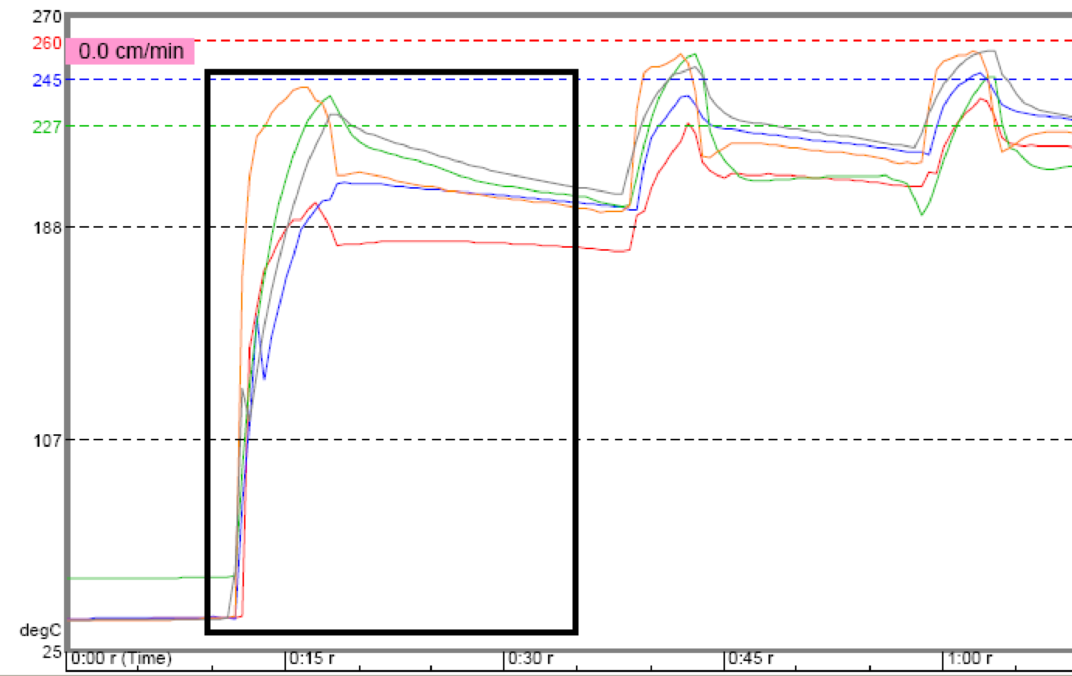
M.O.L.E.(r) STATUS
Max Internal T: 30C
Battery: 4.981
Points: 139

Active: 123456
Interval: 00:00:00.5

Date: 05/13/09
Time: 12:26:02 V09.02

Tool status box





Summary Stats	Peak	Minimum	Max (+)Slope	Max (-)Slope	Time Above 227C	Time 150-180C	227C / Peak	Peak \ 227C
Sensor 1 Location.	237.8	37.2	118.89	-15.00	3.5	1.5	0.53	-10.56
Sensor 2 Location.	247.8	37.2	75.56	-9.44	13.5	3.0	0.93	-3.43
Sensor 3 Location.	255.0	52.8	73.89	-30.00	10.5	1.0	1.05	-1.32
Sensor 4 Location.								
Sensor 5 Location.	256.1	36.7	169.44	-36.11	14.0	0.5	0.60	-19.26
Sensor 6 Location.	256.1	36.7	88.33	-12.22	22.0	1.5	0.64	-5.78
Range	18.3	16.1	95.56	26.67	18.5	2.5	0.52	17.94

Dip Cycle	Dip Time (sec)	Dip ΔT (degC)	Heating Ramp Rate (C/sec)	SS Temperature after Dip (degC)	Cooling Rate (C/sec)
1	25	203C; ambient 37C to 240C in 5 sec	70+	180-195	1.5
2	20	75C; 180 to 255C in 5 sec	30-50	205-220	0.8
3	20	51C;205 to 256C in 5 sec	15-20	Cool to ambient	0.5

Horizontal vs. Vertical Processing

- Vertical Process Preliminary Findings:
  - PCB thermal shock recorded → linking to laminate defects
  - Highly variable; poor finish quality observed, tooling hole clearance issues
  - “Gravity bumps” and uneven plating within PTH barrels observed
  - Uneven PCB exposure times; first in / last out at leading edge

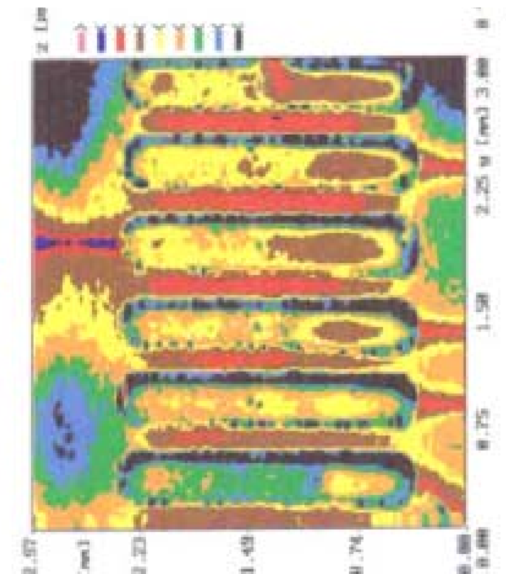
- Horizontal Process Preliminary Findings
  - Slower ramp rates observed
  - Lower thermal exposures
  - Improved flatness consistency
  - Preferred application method for PCB protection

- **Intent:** Examine PCB laminate integrity / reliability after various heat exposures; examine surface finish quality on various design features
- **Status:** PCB fabrication heat exposure in progress; assembly exposures next

- Various PCB Design Features Examined
  - SMT pads (1mm to 0.5mm pitch BGA, SMT DIMM, etc)
  - PTH barrels (various pitch and aspect ratios)
  - Tooling holes, compliant pin geometries

- Processes and Equipment Examined
  - Horizontal vs. Vertical processing
  - 1X through 4X HASL rework operations
  - Multiple HASL tool supplier comparisons

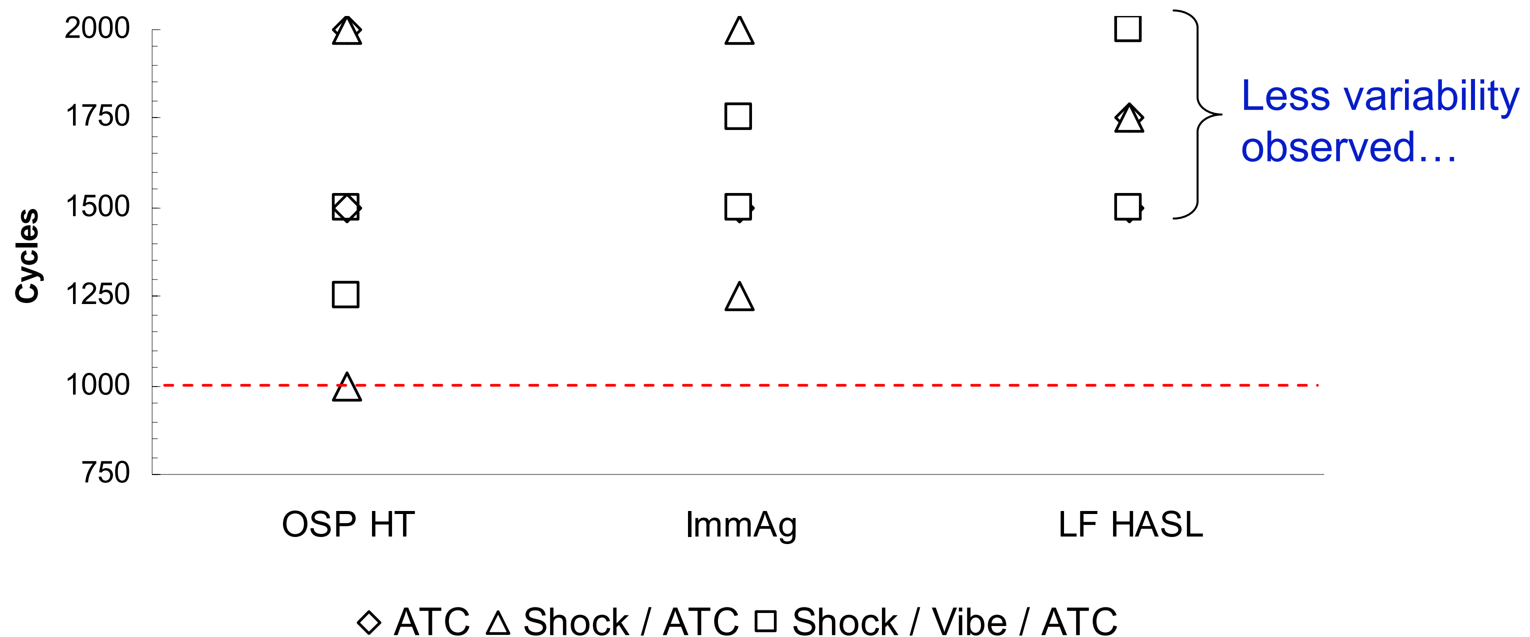
- Laminate Integrity Reliability Testing: Monitored Locations
  - General HASL application and wetting
  - Cu dissolution measurements
  - Uneven plating
  - SMT Pad Flatness Assessment
  - IP Separation / Laminate Cracks
  - Resin Recession
  - Plugged PTH Barrels / Corner Cracking
  - Foil Cracks / Pad Lifting
  - Delamination



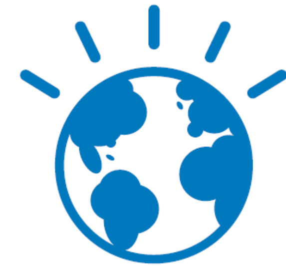
- Follow-on Examination
  - Via Reliability
  - Pad Adhesion
  - Compliant Pin Assessment

- Laminate Integrity After PCB Fabrication — FINISHING
- Laminate Integrity After Electronic Card Assembly — STARTING
- Harsh Environment Corrosion Resistance via SIR — STARTING

- PV 2 Thermo Mechanical Accelerated Cycling Summary — COMPLETE



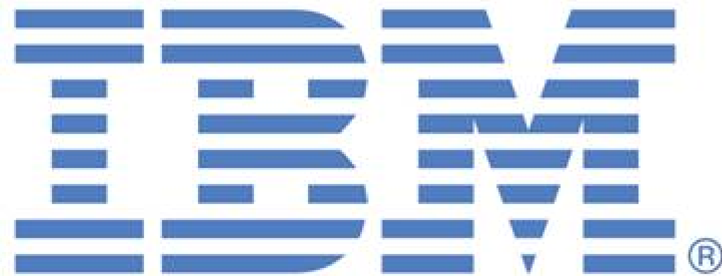
- Functional PV qualification testing yielded excellent results (2007-2008)
  - Second level reliability comparable with OSP
  - Led to additional investigation into merits of HASL
- However, additional technical work required (in progress) to ensure:
  - PCB laminate integrity / reliability
  - High quality final surface finish (controlled)
  - Acceptable yields with various design features / complexities
- Remaining supply chain challenges
  - Switching costs / PCB supplier adoption of horizontal tools (high capital costs)
  - Additional LF HASL studies by other IBM PCB suppliers required
  - Continue with Phases 2 through 5 of strategic plan (BAU manufacturing processes)



Several hurdles yet to overcome…

… but if this surface finish development program is successful, lead-free HASL may be considered as a cost effective surface finish option for high complexity, high reliability IBM Server and Storage products

This is where you, our integrated supply chain can help…



Thank you. Questions?

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