ANALYSIS AND DESIGN OF MASTER/SLAVE CURRENT SHARING
VALIDATED BY CIRCUIT SIMULATIONS

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Current sharing of paralleled power supplies used to achieve higher system reliability

→ each power supply has similar thermal performance

Master/slave current sharing scheme most often used

Design of master/slave current sharing generally not well understood

→ many design pitfalls exist
  • e.g. interconnect impedance between units critical for loop design

Due to its complexity, optimum design not often achieved

→ frequent last minute design changes leads to increased development time/cost
OBJECTIVE

- To obtain physical insight into the dynamics of the master/slave current sharing scheme by analyzing its small-signal behavior
  - determine pole and zero positions relative to components values and operating conditions
- Once pole and zero positions are determined, an optimum design can be obtained
- Before system hardware is developed, validation of analytical calculations (e.g., calculations using Mathcad) should be obtained through circuit simulation (e.g., Pspice, SIMPLIS, etc.)
- Basic operation
- Modeling
  - example circuit
    - phase-shift full-bridge with current mode control
    - relate circuit to block diagram
- Analyze block diagram
  - identify key loop gains
  - design voltage loop compensation
  - design current sharing loop compensation
- Validate design through simulation
  - frequency domain
  - time domain
- Example of poor design
- Conclusion
- Each unit connected in parallel
  - common output voltage $V_O$
  - common current share bus $V_{CS}$
ESTABLISHING MASTER/SLAVE RELATIONSHIP

\[ I_{01} > I_{0k} > I_{0n} \]

- Current-share bus voltage determined by module with highest current (master module)
  \[ V_{CS} = V_{CS1} = V_{CS(MASTER)} \]

- Any module can be master

- In case of failure of current master, one of remaining modules becomes new master
DEFINITION OF FUNCTIONAL BLOCKS – LOCAL SENSING

\[ I_O = f(V_{EA}, V_O) \]
\[ \hat{I}_O = G_1 \hat{V}_{EA} + G_2 \hat{V}_O \]

\[ V_1 = f(V_O, V_{REF}, V_{ADJ}, I_O) \]
\[ \hat{V}_1 = K_d \hat{V}_O + G_{ADJ} \hat{V}_{ADJ} + G_3 \hat{I}_O \]
\[ \hat{V}_{REF} = 0 \]
DEFINITION OF FUNCTIONAL BLOCKS – REMOTE SENSING

\[ I_O = f(V_{EA}, V_O) \]
\[ \dot{I}_O = G_1 \dot{V}_{EA} + G_2 \dot{V}_O \]

\[ V_1 = f(V_O, V_{REF}, V_{ADJ}, V_O) \]
\[ \dot{V}_1 = K_d \dot{V}_O + G_{ADJ} \dot{V}_{ADJ} \]
\[ \dot{V}_{REF} = 0 \quad G_3 = 0 \]
- Multiloop control system
  - voltage loop $T_V$
    \[ T_V = G_{VC} K_d G_{EA} K \]
  - current share loop $T_{CS}$
    \[ T_{CS} = G_{EA} K G_1 G_{CS} G_{CA} G_{ADJ} \]
  - droop share loop $T_D$
    \[ T_D = G_{EA} K G_1 G_3 \]
DESIGNING A MULTILOOP SYSTEM

- Voltage loop
  → requires high bandwidth for good load regulation performance

- Current sharing loop
  → requires high gain at low frequency for good dc current sharing
  → loop bandwidth not critical
    • must ensure stable design

- Separation of crossover frequencies of voltage and current-share loops is necessary to minimize interaction between loops
  → loop interaction causes oscillations in output current of paralleled units

- High bandwidth loops closed first
• Current sharing loop $T_{CS}$ is open

• Loop gain $T_V$ requirements
  - high dc gain for regulation accuracy
  - high loop bandwidth (crossover frequency) $f_{cv}$ for fast dynamic response
  - stable
CIRCUIT DIAGRAM OF TWO UNITS CONNECTED IN PARALLEL

UNIT 1

UNIT 2

V_o

V_{\text{BUS}}

V_{\text{IN}}

V_{\text{CS}}

V_{\text{REF}}

V_{\text{LOCAL}}

V_{\text{BUS}}

V_{\text{IN}}

V_{\text{CS}}

V_{\text{REF}}

V_{\text{LOCAL}}
BLOCK DIAGRAM OF TWO UNITS CONNECTED IN PARALLEL

UNIT 1

UNIT 2

\[ ^\wedge V_o \]

\[ ^\wedge V_{BUS} \]
ESTABLISHING MASTER/SLAVE RELATIONSHIP

\[ V_{\text{VLOCAL}}^s < V_{\text{VLOCAL}}^m \]

SLAVE

UNIT 1

\[ \hat{V}_O \]

MASTER

UNIT 2

\[ \hat{V}_{\text{IBUS}} \]
SIMPLIFIED BLOCK DIAGRAM

\[ V_{\text{ILocal}}^s < V_{\text{ILocal}}^m = V_{\text{IBUS}} \]

SLAVE
UNIT 1

\[ \hat{V}_o \]

\[ G_{VC}^s \]

\[ K_d^s \]

\[ G_{EA}^s \]

\[ G_{CS}^s \]

\[ G_{CS}^s \]

\[ G_{CA}^s \]

\[ V_{\text{ILocal}}^s \]

\[ G_{1}^s \]

\[ G_{3}^s \]

\[ G_{2}^s \]

\[ \hat{V}_{REF}^s \]

\[ G_{adj}^s \]

\[ G_{1}^m \]

\[ G_{2}^m \]

\[ G_{3}^m \]

\[ G_{CS}^m \]

\[ G_{CS}^m \]

\[ G_{SD}^m \]

\[ G_{VC}^m \]

\[ K_d^m \]

\[ V_{REF}^m \]

\[ \hat{V}_{\text{ILocal}}^m \]

\[ \hat{V}_{O} \]

\[ ^\wedge V_{\text{IBUS}} \]

MASTER
UNIT 2
SIMPLIFIED BLOCK DIAGRAM

\[ V_{\text{ILocal}}^s < V_{\text{ILocal}}^m = V_{\text{IBUS}} \]

SLAVE
UNIT 1

\( G_{VC}^s \)

\( K_d^s \)

\( G_{EA}^s \)

\( G_{CS}^s \)

\( G_{CA}^s \)

\( G_{ADJ}^s \)

\( G_{CS}^s \)

\( T_{D} \)

\( T_{CS} \)

\( ^{\wedge} V_{\text{ILocal}} \)

\( ^{\wedge} V_{\text{IBUS}} \)

MASTER
UNIT 2

\( G_{VC}^m \)

\( K_d^m \)

\( G_{EA}^m \)

\( G_{CS}^m \)

\( G_{ADJ}^m \)

\( G_{CA}^m \)

\( G_{CS}^m \)

\( ^{\wedge} V_{\text{ILocal}} \)

\( ^{\wedge} V_{\text{IBUS}} \)

\( ^{\wedge} V_O \)
CURRENT SHARING LOOP GAIN FOR IDENTICAL POWER SUPPLIES WITH REMOTE SENSING

- Identical blocks
- Remote sensing \((G_3 = 0)\)

\[
T_{CS} = G_{CS} G_{ADJ} G_{EA} K G_1 G_{CA}
\]

\[
T_{1}^{RS} = T_{1}\big|_{G_3=0} = -G_{PLANT} G_{CA}
\]

Due to finite open loop gain of \(G_{EA}\)
CURRENT SHARING LOOP GAIN FOR IDENTICAL POWER SUPPLIES WITH LOCAL SENSING

- Identical blocks

\[ T_{CS} = \frac{G_{PLANT}}{G_{CS} G_{ADJ} G_{EA} K G_1 G_{CA}} \]

\[ T_D = G_1 G_3 G_{EA} K \]

\[ T_1^{LS} = -\frac{G_{PLANT}}{1 + T_D} G_{CA} \]

- At breakpoint \( T_1 \)
  \( \rightarrow \) gain significantly higher at low frequency when remote sensing is implemented
  \( \rightarrow \) low frequency poles do not coincide

- Good design practice
  \( \rightarrow \) compensate for remote sensing
• Crossover frequency (bandwidth) of current share loop $f_{CI}$ must be at least one decade (ten times) lower than crossover frequency (bandwidth) of voltage loop $f_{CV}$

$$f_{CI} \ll f_{CV}$$

• Separation of crossover frequencies of voltage and current-share loops is necessary to minimize interaction between loops

→ loop interaction causes oscillations in output current of paralleled units

• Loop gain optimization can only be performed using analytic approach

→ knowledge of pole and zero positions relative to components values and operating conditions is necessary for proper loop compensation

• Validation of loop gain should be done using simulation software prior to hardware development
• Compensation $G_{CA}$
  → current sharing loop bandwidth $f_{CI}$
  1-2 decades below voltage loop bandwidth $f_{CV}$
  → zero placed 2-3 octaves below desired current sharing crossover frequency $f_{CI}$
    • to boost phase margin
  → integrator for good current sharing accuracy
• Compensation $G_{CA}$

$\rightarrow$ local sensing significantly lowers loop bandwidth

$\rightarrow$ crossover with $-1$ slope, ensuring acceptable phase margin $PM$
• Good agreement between analytical calculations and Simplis circuit simulation up to half of switching frequency $f_{SW}$
**VERIFICATION OF CURRENT SHARE LOOP GAIN**  
**FREQUENCY DOMAIN**

- Good agreement between analytical calculations and Simplis circuit simulation up to voltage loop crossover frequency \( f_{CV} \)

**REMOTE SENSING**

![GAIN and PHASE + 180° plots]

- **GAIN** plot shows the gain in decibels (dB) against frequency in Hz.
- **PHASE + 180°** plot shows the phase shift with a +180° notation against frequency in Hz.

Key parameters highlighted:
- \( f_{CV} \) and \( f_{SW} \) labeled on both graphs.
- **PM=76°** marked on the PHASE plot, indicating phase margin.

Analytical and Simulation results are compared, illustrating the agreement between theoretical calculations and simulation outputs.
VERIFICATION OF CURRENT SHARE LOOP GAIN
FREQUENCY DOMAIN

- Good agreement between analytical calculations and Simplis circuit simulation up to voltage loop crossover frequency $f_{CV}$

LOCAL SENSING

**GAIN**

- Local
- Remote
- Analytical
- Simulation

**PHASE + 180°**

- Local
- Analytical
- Remote
- Simulation

$\text{PM}=100°$
VERIFICATION OF CURRENT SHARE LOOP GAIN
TIME DOMAIN

REMOTE SENSING

- Individual output currents shown to converge
  → demonstrates stability
EFFECT OF INTERCONNECT RESISTANCE $R_{\text{INT}}$ ON CURRENT SHARING LOOP GAIN

- As interconnect resistance $R_{\text{INT}}$ decreases, current share loop gain increases at low frequency.

**LOCAL SENSING**

**GAIN**

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<th>Local</th>
<th>Remote</th>
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<td>80</td>
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<tr>
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<td>20</td>
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<tr>
<td>1000000</td>
<td>30</td>
<td>10</td>
</tr>
</tbody>
</table>

**PHASE + 180°**

<table>
<thead>
<tr>
<th>Frequency [Hz]</th>
<th>Local</th>
<th>Remote</th>
</tr>
</thead>
<tbody>
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<tr>
<td>1000000</td>
<td>30</td>
<td>10</td>
</tr>
</tbody>
</table>

$R_{\text{INT}} = 0.5\,\text{mΩ}$

$3.3\,\text{mΩ}$
• Poor loop design
  → Example
    • using traditional 2 pole, 1 zero compensation while filtering current sense signal

→ Local sense
  • stable with excellent phase margin

→ Remote sense
  • unstable with negative phase margin!
EXAMPLE OF POOR DESIGN – FREQUENCY DOMAIN

- Good agreement between analytical calculations and Simplis circuit simulation up to voltage loop crossover frequency $f_{CV}$

LOCAL SENSING
EXAMPLE OF POOR DESIGN – TIME DOMAIN

- Individual output currents
  - stable for local sensing
  - unstable for remote sensing
CONCLUSION

• Detailed knowledge of each power supply essential for proper current sharing loop design

• Design of current share loop gain compensation should be done for remote sensing

• Analytical modeling shown to gain physical insight into pole/zero locations
  → knowledge of pole and zero positions relative to components values and operating conditions is necessary for proper loop compensation

• Simulation tools provide validation of the design which is useful prior to hardware development
f_{SW} = 143kHz  
\( m_c = 2.358 \)  
D = 0.665
APPENDIX

\[
G_{VC} = \frac{R_L}{R_S} \cdot \frac{1}{1 + \frac{R_L}{f_{SW} L_f/2} \left( m_c (1 - D) - 0.5 \right)} \cdot \frac{1 + s/\omega_{zc}}{1 + s/\omega_p} \cdot \frac{1}{1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2}}
\]

\[
\omega_{zc} = \frac{1}{r_c C_f} \quad \omega_n = \pi f_{SW}
\]

\[
Q_p = \frac{1}{\pi (m_c (1 - D) - 0.5)}
\]

\[
G_{CS} = 40 R_{CS} \quad K = \frac{1}{3} \quad K_d = \frac{V_{REF}}{V_O}
\]

\[
G_{EA} = \frac{\omega_1}{s} \left( \frac{1 + \frac{s}{\omega_{z1}}}{1 + \frac{s}{\omega_{p1}}} \right) \quad G_{ADJ} = \frac{R_1 \parallel R_{D2} \parallel R_{D1}}{R_{ADJ}}
\]

\[
\omega_1 = \frac{1}{R_1 (C_{fs} + C_{fp})}
\]

\[
\omega_{z1} = \frac{1}{R_f C_{fs}}
\]

\[
\omega_{p1} = \frac{1}{R_f \frac{C_f C_{fp}}{C_{fs} + C_{fp}}}
\]

\[
G_1 = \frac{1 + \frac{s}{\omega_{zc}}}{R_S \left( 1 + \frac{s}{\omega_{pg1}} \right)} \quad G_2 = \frac{sC_f}{1 + \frac{s}{\omega_{pg1}}}
\]

\[
G_3 = R_{INT} \frac{R_1 \parallel R_{D2}}{R_1 \parallel R_{D2} + R_{D1}}
\]

\[
\omega_{pg1} = \frac{1}{C_f \left( r_c + R_{CS} + R_{INT} \right)}
\]
REFERENCES


