Z-Axis Power Delivery (ZAPD)

Concept and Implementation
The Slew Rate Wall

- **2003**
  - $\frac{di}{dt} = 400 \text{ A/ns}$
  - $V_{\text{droop}} = 110 \text{ mV}$

- **2004**
  - $\frac{di}{dt} = 680 \text{ A/ns}$
  - $V_{\text{droop}} = 100 \text{ mV}$

- **Beyond 2005**
  - $\frac{di}{dt} = 1000 \text{ A/ns}$
  - $V_{\text{droop}} = 75 \text{ mV}$

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- **MB**
- **VRM**
- **Edge Connect**
- **OPVR**
- **ZAPD**

- **500pH**
- **1500pH**
Power Delivery Challenge
Reduction of Path Impedance

3rd Droop
Controlled by VRM & MB filter caps (Bulk & HF)

60 A/us

Capacitance is a Band-Aid. Inductance is the Key.

2nd Droop
Controlled by interposer & pkg caps

100 A/us

1st Droop
Controlled by on-die & pkg caps

1000 A/us

Based on Intel ITS presentation
Distributed Power Architectures
Motherboard Interconnect

Example 32-Bit Processor Power Distribution
(60 A/us max at VRM)

Power Conversion Needs to Move Closer to CPU
Distributed Power Architectures
Edge-Connect Processor Interconnect

Example 64-bit Power Distribution
(100 A/us max at VRM)

Need Modular Power Supply As Close As Possible
The Next Logical Step?  
On-Package-Voltage-Regulation (OPVR)?

- Advantages
  - Power distribution performance
- Disadvantages
  - Non-modularity (embedded w/CPU)
  - VR failures result in CPU failures
- Concept has been around for over 6 years and has yet to take hold due to above.
Power Path Analysis
A Comparison of VRD to ZVRM

VR Down Power Path

ZVRM Power Path
Z-Axis Power Delivery

Fully integrated solution includes:
• Thermal
• Power / Signal Delivery
• Power Delivery to top of processor (Active / Passive)
• Alignment
• Keying
• Retention
• Efficient use of z-axis space
KEY BENEFITS

- Signal Routing separated from Power Routing
- Motherboard real estate consolidation
- A Single integrated heat sink assembly for CPU & Z-Axis circuitry.
- Fast response & tighter voltage variance due to VR proximity (reduced power impedance delivery) = Higher frequencies for CPU. Performance able to support well beyond VRM capability.
- Potentially reduced component count due to reduced power delivery impedance (e.g. fewer capacitors).
- Confirmed designs up to 140 Amps.
Thermal
Z-Axis Power Delivery Thermal Solution

- A single integrated heat sink assembly for CPU & Z-Axis circuitry.
- Z-axis components lie on periphery of heat sink base where thermal performance for CPU is inefficient.

Heat Sink Assembly

100 Watt; 0.255 degree C per Watt
Low Lateral Heat Conduction

CPU

ZVRM FETs

ZVRM FETs

ZVRM Uses Edges of CPU Heatsink which are not Effectively Used Today

ZVRM Thermal Profile

1.3°C

Low Lateral Heat Conduction
A single integrated heat sink assembly for CPU & VR.

**Thermal**

**Mechanical**
- 76mm x 109 mm x 85mm (H x W x L)
- Weight: ~ 500 grams with fan and clips
- Fan: 70 mm; 5400 RPM

**Mechanical**
- 0.256 °C/Watt
- CPU Power Target: 100 Watts
- Form factor changes have allowed sub 0.20 °C/Watt

**Materials**
- Base: Aluminum
- Heat Pipe: Copper
- Fins: Aluminum and Copper
- Processor Thermal Interface: Shin Etsu G751

**Status**
- Sample Shipping
- Drawings available
Thermal Path Analysis
A Comparison of VRD to ZVRM

**ZVRM Thermal Resistance Diagram**

### Thermal Impedance System to Air

\[ \theta_{SA} = \frac{T_{die} - T_{amb}}{P_{die} + P_{ZVRM}} \]
Thermal Test Results

- An 80% efficient ZVRM, full coverage TIM3, and 32.5mm lid increased the case temperature by 2.1°C and die temperature by 2.3°C at 99W. This temperature increase can be reduced, but not yet thoroughly evaluated.

- The 32.5mm small lid had a 0.7°C increase in case temperature and a 0.1°C decrease in die temperature compared to the 37.5mm large lid package. Since this test requires the use of two different thermal sources.

- The ZAPD power connectors had less than a 13°C temperature increase from no ZVRM DC load to an 80% efficient ZVRM at 99W (65A).

- The ZVRM FETs had less than a 44°C temperature rise from ambient at 99W and 80% efficiency.
Voltage Regulation
Z-Axis Power Delivery with Voltage Regulation (Optional)

- Fast response & tighter voltage variance due to VR proximity (reduced power impedance delivery) = Higher frequencies for CPU. Performance able to support well beyond VRM capability.
- Potentially reduced component count due to reduced power delivery impedance (e.g. fewer capacitors).
- A multi-phase DC-DC converter using traditional buck topology & industry standardized components.
- Confirmed designs up to 140 Amps.
Substrates
Proposed Substrate Modifications for ZAPD
Thermal Load Board

- Emulates the CPU/substrate thermal load.
- Verifies the thermal simulation results and serves as a stand alone DC load
- Calibrated etched resistor on a polyamide PWB powered by the ZVRM.
- Produces and accurately measures 78 to 101 watts of uniformly distributed heat.
Silicon Thermal Test Die – STTV
Validate Package/Substrate w/ ZVRM

- Demonstrate thermal, electrical and mechanical performance of the package in the ZVRM configuration
  - STTV including BUM substrate, modified lid and C4 thermal die array
  - Test MoBo with socket

- Package Testing
  - Characterization / Analysis / Reliability Assessment

- Can selectively heat 16 locations

4 x 4 Thermal Die Array for STTV
Thermal Power Testing
CRTV – Contact Resistance Test Vehicle

**Mechanical**
- Substrate Dimension: 40mm x 40mm
- Lid Dimension: 32mm x 32mm

**Electrical**
- 16 zone thermal element
- 4-point Contact Resistance Test configuration

**Materials**
- Top Pads: 30u” Electroplated Au over 120 u” Nickel

**Features and Benefits**
- Designed to test contact resistance of Power Interconnect (Molex Series Number: 64887-001)
- Mimics mechanical load of typical microprocessor.
- Fabricated by NTK
- Fits into standard uPGA connectors

CRTV – Contact Resistance Test Vehicle – Used to evaluate contact resistance changes in the system.
Interconnect
Z-Axis Power Delivery Interconnect

**Features and Benefits**
- Power to the “Top” of the Processor
- Separate voltage source (VR or passive interconnect)
- Uses high-current interconnect to contact surface of CPU pkg to support growing DC current.
- Low impedance power delivery path to the microprocessor to support growing dynamic AC current changes of CPU (2nd order droop reduced).
- 68 pH (34 pH design available, 15 pH designs modeled)
- Originally designed for power, but could be used for signals
- Connector designed to compensate for Z-Axis tolerances.

**Mechanical**
- Vertical Compliance: 0.7 mm
- Contact Force: ~90 grams avg.
- Durability: 25 Cycles

**Electrical (Quad-Array)**
- Loop Inductance: 68 pH
- Total Current Target: 80 Amps

**Materials**
- Terminal: Phosphor-Bronze
- Housing: LCP
- Contact Plating: 30 μ" Au over 50 μ" Nickel
- SMT Tail Plating: Tin-Lead

**Status**
- Sample quantities available
- Drawings available
Phase II and Phase III Connectors

- Lower Inductance
  - 140 Amps

- Lower Cost
  - 80 Amps

- 200 Amp Modeled
Mechanical Simulation

Material:
Beryllium Copper C17460 HT
Thickness = 0.127 mm
Interference Height : 0.71 mm
Normal Force : 108 grams
Interconnect AC Inductance Test

- Design verification vehicle to determine inductance and AC resistance.
- Confirms modeling calculations from design phase
- Uses the $S_{21}$ measurement technique with a network analyzer.
Connector Inductance

Simulation
DC Contact Testing
Test Fixtures

TOP BOARD

BOTTOM BOARD

CRTV
## Test Groups

<table>
<thead>
<tr>
<th>A) EIA-364 TS-1000.01 Temp and Humidity: Test Group 2</th>
<th>B) EIA-364 TS-1000.01 Vibration: Test Group 3</th>
</tr>
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<tbody>
<tr>
<td><strong>Low Level Contact Resistance:</strong> EIA-364-23</td>
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</tr>
<tr>
<td><strong>Durability (Preconditioning):</strong> EIA-364-09</td>
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</tr>
<tr>
<td>5 plug / unplug cycles</td>
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<tr>
<td><strong>Thermal Shock</strong></td>
<td><strong>Temperature Life:</strong> EIA-364-17: Mated</td>
</tr>
<tr>
<td>10 Cycles: -55 °C to +85 °C: Mated</td>
<td>105 °C / 240 hours</td>
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<tr>
<td><strong>Cyclic Temperature and Humidity</strong></td>
<td><strong>Vibration Schedule:</strong></td>
</tr>
<tr>
<td>25 °C at 80% humidity to 65 °C at 50% humidity</td>
<td>• 20 –500 Hz</td>
</tr>
<tr>
<td>Ramp: 0.5 hours</td>
<td>• 3.1 G</td>
</tr>
<tr>
<td>Dwell: 1 hour</td>
<td>• Random PSD</td>
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<tr>
<td>Cycles: 24</td>
<td>• 15 minutes per axis duration</td>
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<tr>
<td><strong>Low Level Contact Resistance:</strong> EIA-364-23</td>
<td><strong>Low Level Contact Resistance:</strong> EIA-364-23</td>
</tr>
<tr>
<td><strong>Durability (Reseating):</strong></td>
<td><strong>Vibration Schedule:</strong></td>
</tr>
<tr>
<td>3 plug / unplug cycles</td>
<td>• 20 –500 Hz</td>
</tr>
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<td><strong>Low Level Contact Resistance:</strong> EIA-364-23</td>
<td>• 3.1 G</td>
</tr>
<tr>
<td><strong>C) Shock</strong></td>
<td>• Random PSD</td>
</tr>
<tr>
<td>• Low Level Contact Resistance: EIA-364-23</td>
<td>• 15 minutes per axis duration</td>
</tr>
<tr>
<td>• EIA-364-27B Shock Test</td>
<td><strong>D) Retention Force:</strong></td>
</tr>
<tr>
<td>• 50G</td>
<td>Measure static force of retention hardware (...</td>
</tr>
<tr>
<td>• 11mS half-sine</td>
<td>(frame, heatsink and clips) using supplied</td>
</tr>
<tr>
<td><strong>E) Contact Beam Force vs. Displacement</strong></td>
<td>fixture.</td>
</tr>
</tbody>
</table>
Contact Resistance Evaluation
Temp Rise

Top

Bottom

Thermal Couple soldered to terminal base
Temperature Rise Chart

- Signals
- Power Path Pins
- Return Path Pins
- Thermal Couple Locations

- VRM PCB
- Bank 1
- Bank 2
- Bank 3
- Bank 4

POWERED: Bank 1
ELECTRICALLY ISOLATED: Banks 2, 3, and 4

Tr6209 Temperature Rise Profile on P2P, Specimen #1

- WORST Case sample results
- Worst Case Location: Outer locations ~ 5º less
- No Heatsink / No Fan / Closed “still air” room
- Load: 1 Oz. Copper across “Bank 1”
- 4 Banks x 35 Amps per Bank = 140 Amps
System Level Power Path Modeling
System Level Analysis

- **VRD**: Voltage Regulator Down
  - As seen in most desktop PCs today
  - Voltage regulator is soldered on to the motherboard.
- **VRM**: Voltage Regulator Module
  - As seen in many servers today
  - Voltage regulator is added to system in the form of a module
  - Typically, module is inserted into an edgecard connector
- **ZAPD**: Z-Axis Power Delivery
  - How does Passive and Active ZAPD systems compare to VRD and VRM
  - System level analysis of VRD, VRM, Passive ZAPD and ZVRM
VRM System
Compare Results: Power Path Impedance

S22

[mOhm]

Frequency [MHz]

3rd order droop - VR Cap
2nd order droop - Inductance
1st order droop - Substrate Caps

ZVRM
NZVRM
VRD & VRM

100.0
10.0
1.0
0.1
0.01
0.10
1.0
10.0
100.0
1000.0
System Testing
ZVRM Voltage droop

Five parts tested, average magnitude of the Hump = 162.8mV

VRD High Hump Running Stopclk & TZ009005

Reference design High Hump Running Stopclk & TZ009005

Five parts tested, average magnitude of the Hump = 88mV

VRD Low Hump Running Stopclk & TZ009005

Reference design Low Hump Running Stopclk & TZ009005

Five parts tested, average magnitude of the Hump = 94.4mV from the VID setpoint, 60mV from onset of transient.
System Testing
Overshoot Comparison Graph

**Spike Voltage Variance Overshoot**

- VRD Only: 84
- Active ZAPD Only: 58
- Passive ZAPD: 58

ZVRM = 45%
Improvement over VRD

**Hump Voltage Variance Overshoot**

- VRD Only: 162.8
- Active ZAPD Only: 68
- Passive ZAPD: 68

ZVRM = 139%
Improvement over VRD
KEY BENEFITS

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