Chip Package Challenges

Jerry Bartley
Quotes to remind you of your perceived limits

“I think there is a world market for maybe five computers.”
Thomas Watson, chairman of IBM, 1943

“Computers in the future may weigh no more than 1.5 tons.”
Popular Mechanics, 1949

“There is no reason anyone would want a computer in their home.”
Ken Olsen, founder of DEC, 1977

“640K ought to be enough for anybody.”
Bill Gates, 1981

“Prediction is difficult, especially about the future”
Yogi Berra
Moore’s Law (Predicting the future….)

CPU Transistor Counts 1971-2008 & Moore’s Law

Curve shows ‘Moore’s Law’: transistor count doubling every two years
Trends in Heat flux

- Future CMOS
- Oxy-acetylene torch
- Hot CMOS chip
- 100 W light bulb
- Surface of sun
- Black body radiation

Heat Flux (W/cm²)

Temperature (K)

- 100000
- 10000
- 1000
- 100
- 10
- 1
- 0.1
- 0.01

- 10
- 100
- 373 K (100 C)
- 1000
- 10000
- 100000

10/20/2009
Power Dissipation Trends

Problems:
- Power Delivery
- "Max" Power
- "Avg" Power

Intel Data
SIA Projection

Nuclear Reactor
Hot Plate
Pentium III
Pentium II
Pentium Pro
Pentium
386
486

Power Density (W/ cm²)

1000
100
10
1

1980 1990 2000 2010
Challenges

Power, Cooling and Frequency Limits

Server microprocessors cannot simultaneously utilize all their transistors due to power limitations.

- Moore’s law is continuing with respect to transistor density, although at a reduced pace, because:
  - Passive Power (power leakage) approaches Active Power
  - Air cooling is pushed to its limits
  - To satisfy power, frequency, and cooling constraints - new materials and methods will be developed

### Active vs Passive Power

<table>
<thead>
<tr>
<th>Year</th>
<th>Active Power (W/cm²)</th>
<th>Passive Power (W/cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1994</td>
<td>0.01</td>
<td>0.01</td>
</tr>
<tr>
<td>2005</td>
<td>1000</td>
<td>100</td>
</tr>
</tbody>
</table>

### Power, Frequency, Cooling Limits

- **Power with Leakage**: Shippable Parts
- **Cooling/Power Limit**: Minimum Ship Frequency
- **Number of Parts**:
  - **Max Freq (No Leakage)**:
  - **Max Freq (With Leakage)**:

**Advanced Cooling Techniques**

- **Air cooling** is being extended through advanced thermal interface materials (TIMs)
- **Copper based liquid cooler**
- **Liquid cooled Apple machine**
- **Power Mac G5**
- **Liquid cooling enables**:
  - High power density
  - Lowering junction temperatures
  - Compact system packaging

Power Density (W/cm²)
The Curve of Change

1. There are more people alive today... than all the humans who have ever lived since the dawn of civilization.

2. 99% of all the scientists who have ever lived... are alive today.

Source: The Gary Hilbert Letter
http://www.thegaryhilbertletter.com/newsletters/population.htm
High Level Definition/Design
(Managing the application variables)

- Functional requirements (what does it have to do?)
- Schedules, resource requirements
- Cost targets (including take-down over time)
- Electrical (Signaling, modeling, noise, power, etc.)
- Mechanical
- Thermal
- Reliability goals, requirements, service/warranty strategy
- Technology selection (criteria, risks, NRE)
- Card and Board layout, structure
- Procurement environment (number of suppliers?)
- Assembly process requirements
- Design margin requirements
- First level packaging (technology selection, risks, NRE)
- Connectors (size, shape, performance, models)
- Test coverage
Wavelength Worries

Wavelength = speed of light / frequency
(in FR4...)

\[ \frac{\lambda}{4}: \quad 365 \text{ m} \quad 36.5 \text{ m} \quad 3.65 \text{ m} \quad 36.5 \text{ cm} \quad 3.65 \text{ cm} \quad 3.65 \text{ mm} \quad 365 \text{ um} \]

- 0.1 MHz
- 1 MHz
- 10 MHz
- 100 MHz
- 1000 MHz
- 10 GHz
- 100 GHz

Datacenter interconnect
Rack
Card-to-card interconnect
Trace lengths
Power shapes
High-end board thickness
Connector features
Package traces
Power shapes
Component attach

Scary in current technology
Channel structure at the Fundamental Frequency

- Impedance match/reflectios
- Detailed timing/delay
- “Few-drop” nets (60x, PCI)
- Common-clock

- Board/Package process variations
- Attenuation dominated
- Point-to-point differential (HSS, PCIE)
- Reference/Recovered clock
- Pattern restrictions

- Simple RLC models
- RLC discontinuities
- Lossless T-lines
- Staged RLC discontinuities
- Coupled lossy T-lines

- Board/Package process variations
- Group matching
- Point-to-point nets (DDRx, HT, PCIx)
- Source-synchronous groups

- 3D fully-extracted channel features

**Time parameters**

- $Z_0 = 50 \, \Omega$
- $T_0 = 40\,\text{ps}$
Building a square wave with Sine/Cosine waves
Transition to 3D CMOS

Year of Announcement

Module Heat Flux (watts/cm²)

Bipolar

CMOS

Opportunity for 3D Si

Challenges
Emerging 3D Silicon Integration

- Another way to extend Moore’s Law
3D Structures and Cooling Approaches

- Chips on a Si carrier
  - Have direct access to the back of each chip
  - Mechanical issues predominate over thermal issues
  - Must develop a very good thermal interface material thick enough to handle chip non-planarity

- Stacked chips of moderate power
  - Can be cooled from the back of the stack
  - Must improve conductivity through complex stack with many thermal interfaces

- Bring cooling into the stack
  - Far more complex, but might allow higher stacks
Thru – Silicon Vias (TSV)

A TSV, before filling

2-layer stack

4-layer stack

C4

3D Chip

Laminate package

Chip: ~730µm

Si P+ ~ 90µm

50-90µm

Ceramic or Organic Substrate
Chimp off the old block

0.6% Really does make a difference !!!!!!

DETAILS REALLY MATTER !!!!!!!!
More Thermal Reality

Detailed knowledge is important

- Understanding the power density
- Understanding the impact of higher Temperatures
- Having the ability to bring the appropriate amount of technology to the application.

<table>
<thead>
<tr>
<th>Tambient (°C)</th>
<th>Tj_nom (°C)</th>
<th>effective hot-spot R (°C/W)</th>
<th>fin base HTC (W/m²K)</th>
<th>TIM1 interface condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>57.5</td>
<td>0</td>
<td>755</td>
<td>uniformly heated chip</td>
</tr>
<tr>
<td>25</td>
<td>64.1</td>
<td>0.15</td>
<td>755</td>
<td>best can-do grease</td>
</tr>
<tr>
<td>25</td>
<td>91.9</td>
<td>0.76</td>
<td>755</td>
<td>2 mil PCM interface</td>
</tr>
</tbody>
</table>
Characteristics of today’s Silicon

Transistor Leakage Vs. Channel Length - nA of leakage vs. Transistor Length (nm)

Total Die Power vs. Vdd by Tj

Die-Level Leakage Power vs. Temperature

Die Static Power (mA)
Observations

- We currently are not able to utilize all of the transistors and capability we can build within the Silicon
- Power in… and Power out… among the key limitations
- Circuit designs, chip materials…. Timing, reliability, yield all pressuring our analysis capability.
- More and more analysis necessary with much higher detail, trade-offs required to achieve success.
- Power structure likely requires more extendibility
- Limitations starting to engage broader teams and disciplines
  - Silicon process, Chemists, etc.
  - System and micro-architecture
  - Device/transistor designers
My Conclusion, Prediction, and Encouragement

- Thermal limitation awareness has become pervasive across all facets of the electronic industry and thus the opportunity for this group to influence the direction of the industry has clearly increased.

- More analytical capability will be required to provide the detail necessary to guide developers (including the other disciplines) toward optimization.

- More interaction to close the gaps between the disciplines will provide large paybacks in the ability to integrate and deploy applications to the marketplace.

- Challenges exist at all levels, we must evolve to succeed.