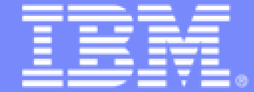
Integrated Supply Chain



PCB Temperature Compatibility with Lead-Free Soldering

Jeffrey Taylor, Marie Cole, Matt Kelly,
Wai Ma, John Wilson

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Agenda

- **IBM Lead-free Transition Roadmap**
- **Lead-free Assembly Requirements for PCBs**
- **PCB Lead-free Qualifications**
- **PCB Lead-free Surface Finishes**
- **Summary**

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IBM Lead-free Transition Roadmap

- **IBM progressing in Lead-free soldering for Servers since 2009**
  - High volume System x and Blades in 2009
  - High end System x and Tape Storage in 2010
  - Select cards in Power Blades, Low End and Mid-Range in 2011
- **Server exemption for lead-free solder may expire in the future**
  - 2010 exemption review recommended a 2014 expiration date
  - Current Recast of the RoHS directive includes a validity period for this exemption until 2016
  - Continue to extend lead-free soldering capability across IBM Server and Storage portfolio

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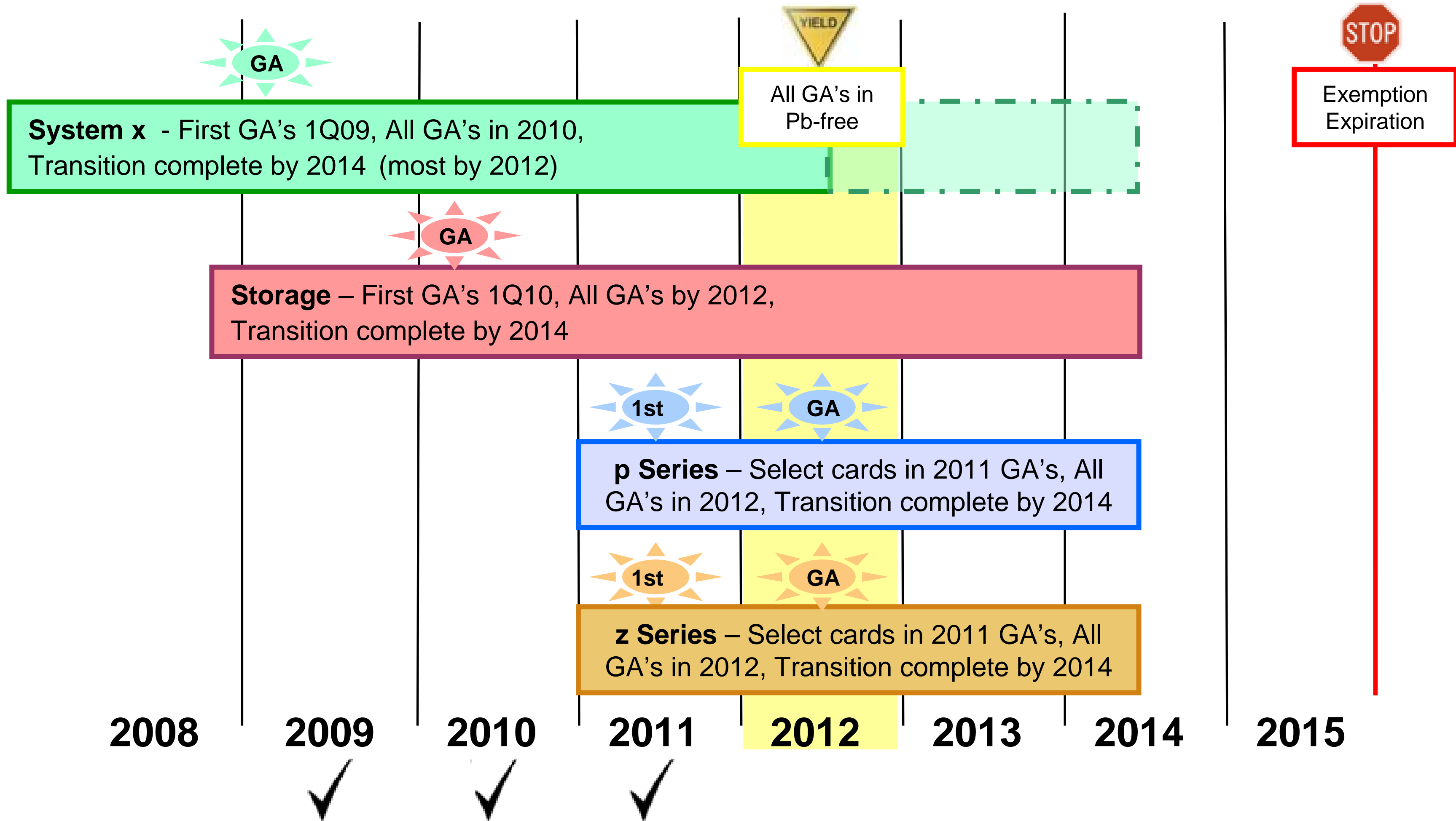
IBM Lead-free Transition Roadmap



PCB raw card must be available for Power-On and qualified for GA (including 260°C)

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Lead-free Assembly Requirements for PCBs

- **Lead-Free PCB Reflow Compatibility**
  - Assembly temperature constraints
    - Minimum solder joint temperature of 230C required for all solder joints in SAC assembly process
    - Maximum component body temperatures: typically 230C – 260C
    - Maximum PCB temperature range of 245C – 260C for SAC primary attach & rework assembly processes
  - Simulated assembly exposures have been developed for PCB qualifications
    - Does not directly correspond to actual thermal exposures of product cards
    - Simulates the cumulative thermal stress of actual exposures
    - Simplified protocol facilitates implementation at PCB suppliers without logistic or capability constraints
  - Most lead-free PCBs reach a 245 ^{o}C peak reflow temperature
    - Don't assume that because a card requires wave soldering or because a particular rework temperature exceeds 245 ^{o}C that the simulated assembly peak temperature will need to be qualified at 260 ^{o}C
    - Remember: "cumulative thermal stress exposure"

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Lead-free Assembly Requirements for PCBs

- **Assembly processing effects**
  - Maximum PCB temperature required is a function of complexity
    - Pin density and thermal mass (components / connectors)
    - SMT complexity
    - PTH complexity
    - PCB construction: thickness, power planes, thermal reliefs, etc
  - Preconditioning must assure primary attach and rework
  - Assembly team continuing to monitor PCB temperatures
    - Ensure qualification limits are met
    - Increased data base across broad set of assemblies
    - Develop predictive tool for PCB reflow temperature required

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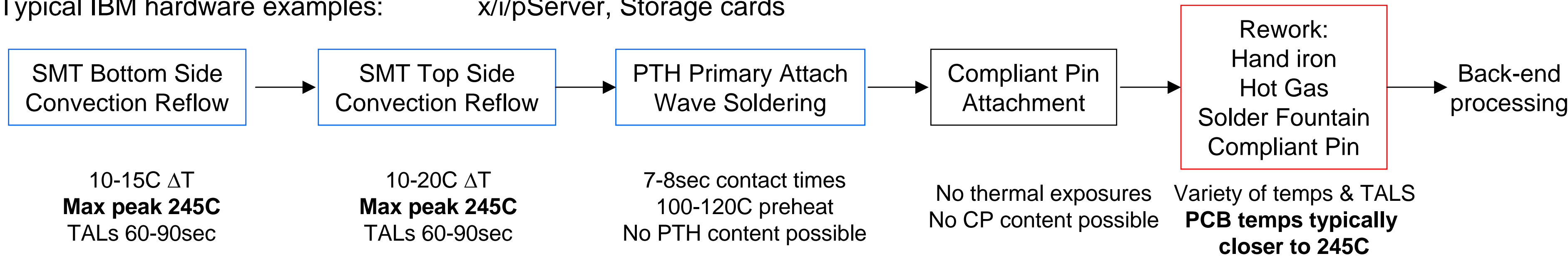
Typical ECAT Lead-Free Thermal Assembly Process Exposures

Actual (simplified) process flows used across IBM WW manufacturing locations

Global heat exposure
Local heat exposure

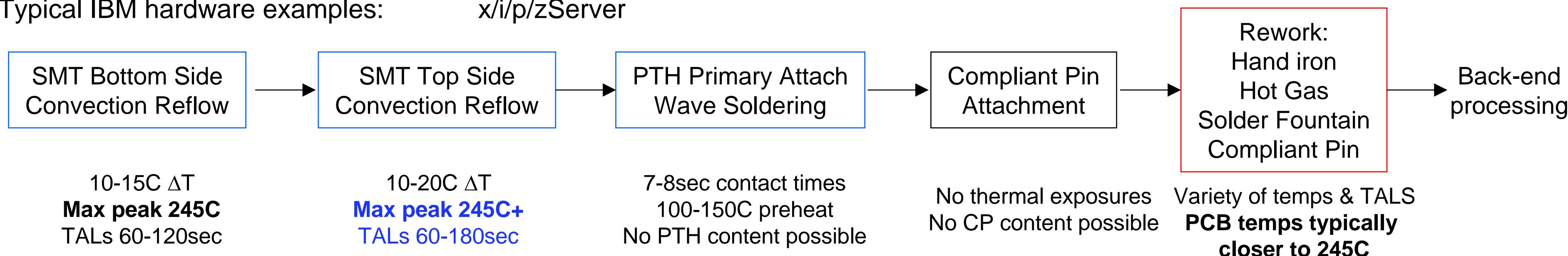
Option 1: Low / Med Complexity Assemblies

Card Thickness range: 0.062” – 0.110”
Card x/y Dimension range: 6”x4” – 15”x17”
Assembly fixturing required: SMT & PTH pallets
Typical IBM hardware examples: x/i/pServer, Storage cards



Option 2: Med / High Complexity Assemblies

Card Thickness range: 0.110” – 0.130”
Card x/y Dimension range: 8”x10” – 18”x20”
Assembly fixturing required: SMT & PTH pallets, minimal load head fixtures
Typical IBM hardware examples: x/i/p/zServer



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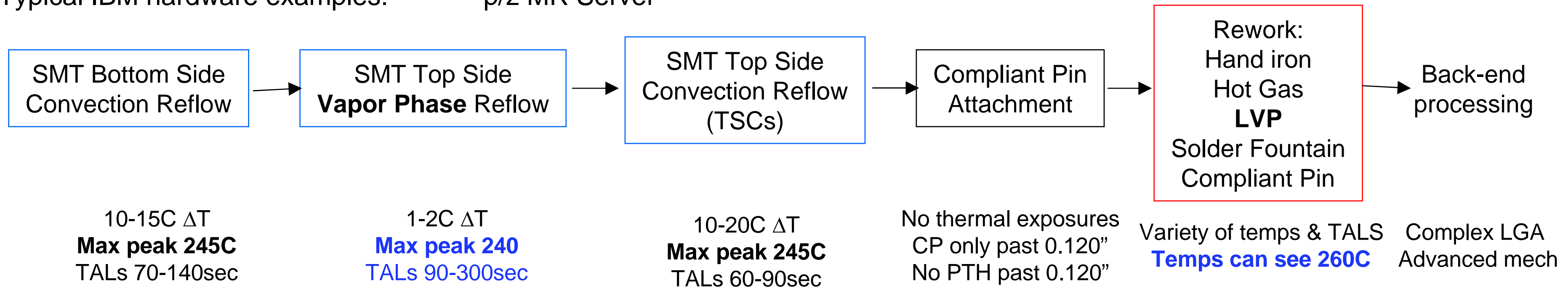
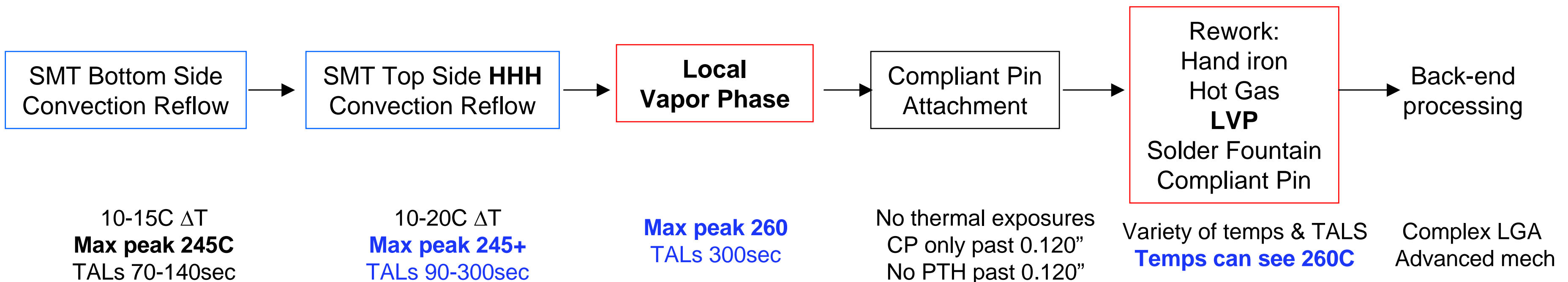
Option 3: High / Ultra High Complexity Assemblies

Card Thickness range: 0.120" – 0.240"
Card x/y Dimension range: 16"x18" – 18"x24"
Assembly fixturing required: SMT & PTH pallets, multiple load head fixtures
Typical IBM hardware examples: p/z MR Server



Option 4: High / Ultra High Complexity Assemblies

Card Thickness range: ~0.250"
Card x/y Dimension range: 16"x18" – 18"x24"
Assembly fixturing required: SMT & PTH pallets, multiple load head fixtures
Typical IBM hardware examples: p/z HE Server



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Simulated Lead-Free Thermal Assembly Process Exposures for PCB Qualifications

- Protocol uses simplified preconditioning process / equipment set for logistics & throughput reasons
- Simplified pre-conditioning process allows for increased PCB supplier test capability
- Known differences and gaps with actual vs. simulated exposures
- PCB pre-conditioning protocols have been designed as worse case exposures
- Protocol focuses on cumulative heat exposure effects (global and local)
- Simulations only use SMT reflow ovens (global heat exposures) to mimic both types of exposures
- Protocol is not perfect but tries to balance actual assembly exposures with logistics and supplier capabilities

Simulation Option 1 applies to assembly options 1 & 2
Simulated exposure: 3X 245C + 2X 245C

Explanation: 3X 245C global exposures cover bottom/top convection SMT + wave processes
2X 245C global exposures cover 2X localized rework operations

---

Simulation Option 2 applies to assembly option 2
Simulated exposure: 3X 260C + 2X 245C

Explanation: 3X 260C global exposures cover higher complexity bottom/top SMT + wave processes
2X 245C global exposures cover 2X localized rework operations

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Simulated Lead-Free Thermal Assembly Process Exposures for PCB Qualifications

Simulation Option 3 applies to assembly option 3
Simulated exposure: 2X 245C + 1X 240C + 2X 260C (higher temperature driven by Ventura LVP rework)

Explanation:
2X 245C global exposures cover complex bottom/top SMT + wave processes
1X 240C global exposure covers top SMT vapor phase process
2X 260C global exposures cover 2X localized rework operations, such as LVP rework

---

Simulation Option 4 applies to assembly option 4
Simulated exposure: Convection + Local Vapor Phase Attach and Rework
2X 245C + 5X Local Vapor Phase (14 row connector) +
2X Hot gas site dress (14R connector) + 6X Hot Gas (8 row connector)

Explanation:
2X 245C exposure covers bottom and top SMT convection global exposure
5X LVP exposures cover LVP primary attach and 2X reworks for 14 row connector
2X Hot gas exposures cover site dress exposure (14 row connector)
6X Hot gas exposures cover local 2X reworks for 8 row connector
(includes 2X site dress thermal exposure)

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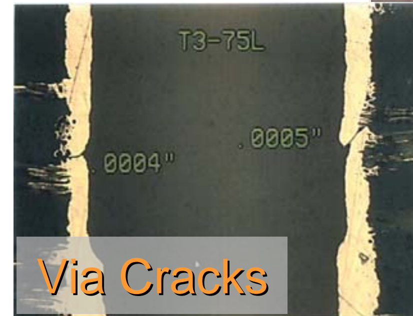
PCB Integrity Tests

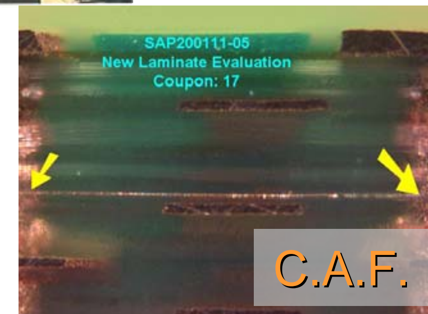
Laminate Integrity

- **Surface-Visible Delamination**
  - Usually in Featureless Areas
  - May Worsen with Storage
- **Hidden Laminate Cracks**
  - Found in Laminates down to 75 mils thick.(thus far)
  - Near Center of Stack Up, No Hint on Surface
  - In Module Sites, within the Laminate
    - At Glass-to-Resin Interface or in the Resin
    - Horizontal or Vertical Cracks



Via Reliability

- Laminate Cracks Invalidate Test
- Candidate Laminate Recipes Meeting Requirements (245°C)
- Failures Due to Various Manufacturing Defects
- Expect Greater Sensitivities as Increase Reflow Temperature



Conductive Anodic Filament Formation

- Laminate Cracks Invalidate Test
- Testing Issue: Acceleration Requires Moisture

Land-to-Barrel Interface Integrity

- More Failures Observed After Reflow than After 6x Solder Float

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Lead-free PCB Qualifications – **2009 Status**

Supplier (Facility / Material)	Thickness (mils)	Peak Temperature		Entry Level	Qualification Status
		245C	260C		
1 / C	75	x		x	Qualified
2 / H		x		x	Qualified
7 / B		x		x	Qualified
9 / L		x		x	Qualified
2 /G	100	x			Qualified
4 / I		x			Qualified
9 / E		x			Qualified
3 /G		x			In Progress
1 / C		x			In Progress
8 /C			x		Investigation
8 /M			x		Investigation
1 /C	110		x		Investigation
2 /G			x		Investigation
9 /L			x		Investigation
5 / J	120	x			Qualified
5 / K			x		In Progress
6 / A	130	x			Qualified
9 / L		x			Qualified
10 / A		x			Qualified
2 /D			x		Investigation
2 /F			x		Investigation
9 /D			x		Investigation

Note:
standard loss laminates

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Lead-Free PCB Qualification Progress – Standard Loss

Material	Mainstream 245 oC	Ruby_100 245 oC	Ruby_110 260 oC	Ruby_130 245 oC	Ruby_130 260 oC	Convection 3X, 245 oC + 2X, 260 oC	Vapor Phase + Convection 2X, 245 oC + 1X, 240 oC + 2X, 260 oC
C1				x		x (150)	
D1	x						
D2			x		x		
D3	x	x	x				
E1		x					
E2				x (150)	x	x (150)	x (170)
F1		x	x			x (110)	
F2	x						
G1					x		
H1		x					
H2			x		x (120) x (130)	x (120)	
H3				x (120)			
J1	x		x	x			
J2		x					

Complete

Under Investigation

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Lead-Free PCB Qualification Progress – Mid and Low Loss

	Material	Low Halogen?	Mainstream 245 oC	Ruby_110 245 oC	Ruby_110 260 oC	Ruby_130 245 oC	Ruby_130 260 oC	Convection + Local Rework 2X 245C + 7x LVP: 14R + 6x HG: 8R
Mid Loss	A1			x				
	A2					x		
	C2					x (137)		
	H1	Y		X (90)				
	I4	Y	x					
	I5	Y		x				
	I6	Y				x		
	J3	Y		x (90)				
Low Loss	B1	Y			x			
	H2			x (110) x (120)				
	J4					x (130) x (150)		
Very Low Loss	H3							x (250)

Complete   Under Investigation   In Progress

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High End Laminate Lead-free Vapor Phase Study

- Micro-Section Results
  - No thermally induced damage found for the following boards:
    - p/z HE, 202 mils, material H3
    - p/z HE, 201 mils, material H3
    - p/z HE, 184 mils, material E1
    - p Mid-range, 173 mils, material E2
  - Thermally induced damage found for the following boards:
    - p/z HE, 204 mils, non-Pb-free material: Laminate cracks
    - p/z HE, 184 mils, non-Pb-free material: Blisters (2), Minor voids
    - p Mid-range, 173 mils, material C1: Laminate & barrel cracks
    - I/O drawer, 86 mils, 3 oz Cu, non-Pb-free material: Laminate cracks
    - I/O drawer, 135 mils, 4 oz Cu, non-Pb-free material: Laminate cracks
- Flatness / Thickness Variation Measurement Results
  - Mitutoyo CMM Tool used for all measurements
  - Measurements taken before and after reflow simulation
  - No significant flatness or thickness variation deltas due to lead-free assembly processing
- Conclusions
  - Laminate cracks expected for those cards tested in non-Pb-free compatible materials
  - 173 mil thickness exceeds the capability of material C1, material E2 required

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Lead-Free Vapor Phase Study

- Assumptions
  - Run trials using available products only
  - Main technology gap will still occur after this testing is completed. Need to bridge to new zHE products
- Objectives
  - Subject various HE PCB raw cards to elevated LF vapor phase reflow processing
  - Close experience gap between 245/260C rated laminates and high complexity, high reliability laminates
  - Develop lead-free VP laminate preconditioning method

System	Laminate	Finish	Card Dimensions	Thickness (mils)	(1) Flatness Measurement	(2) LPAT Reflow Precondition	(3) Flatness Measurement	(4) Hipot Test	(5) Microsection
p/z HE	H3	OSP	23.061" x 14.346"	202	X	X	X		X
p/z HE	non-Pb-free	OSP	25.472" x 16.594"	204		X		X	X
p/z HE	H3	OSP	21.417" X 19.055"	201		X			X
p/z HE	non-Pb-free	OSP	21.417" x 16.811"	184	X	X	X		X
p/z HE	E2	OSP	21.417" x 16.811"	184	X	X	X		X
p Midrange	C1	OSP		173	X	X	X		X
p Midrange	E2	OSP		173	X	X	X		X
I/O Drawers	non-Pb-free	OSP	22.446" x 6.566"	86		X			X
I/O Drawers	non-Pb-free	OSP	22.047" x 6.371"	135		X			X

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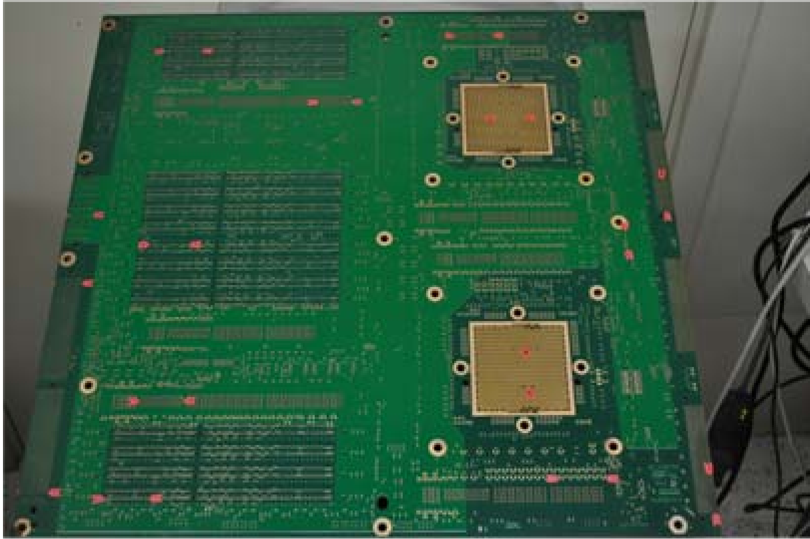
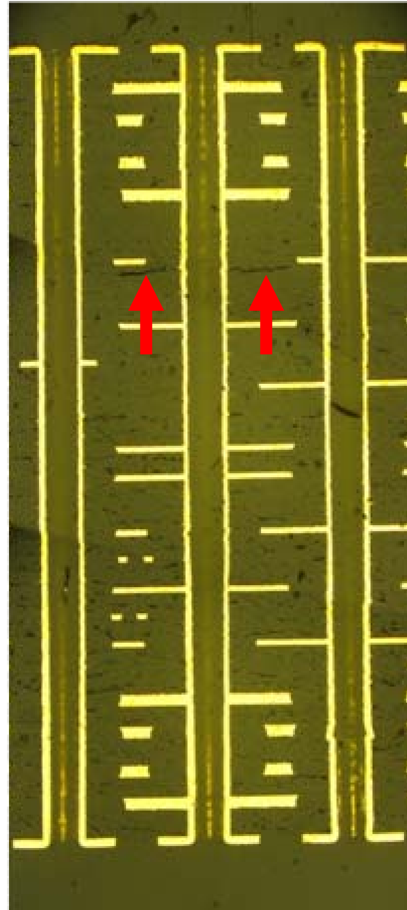
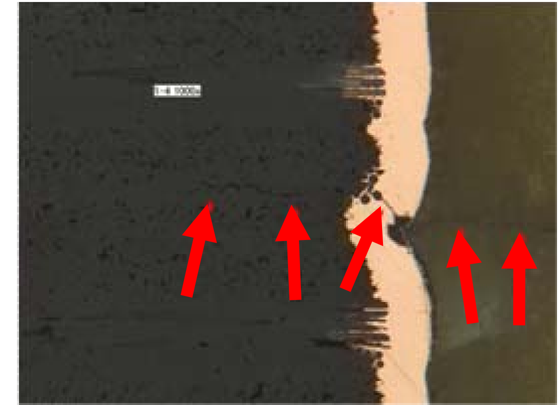
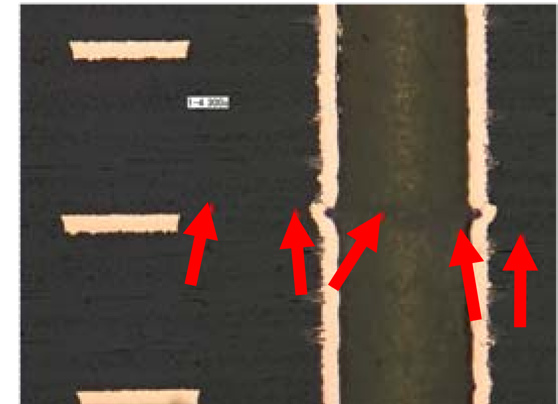
p Mid-range, 173 mil thick









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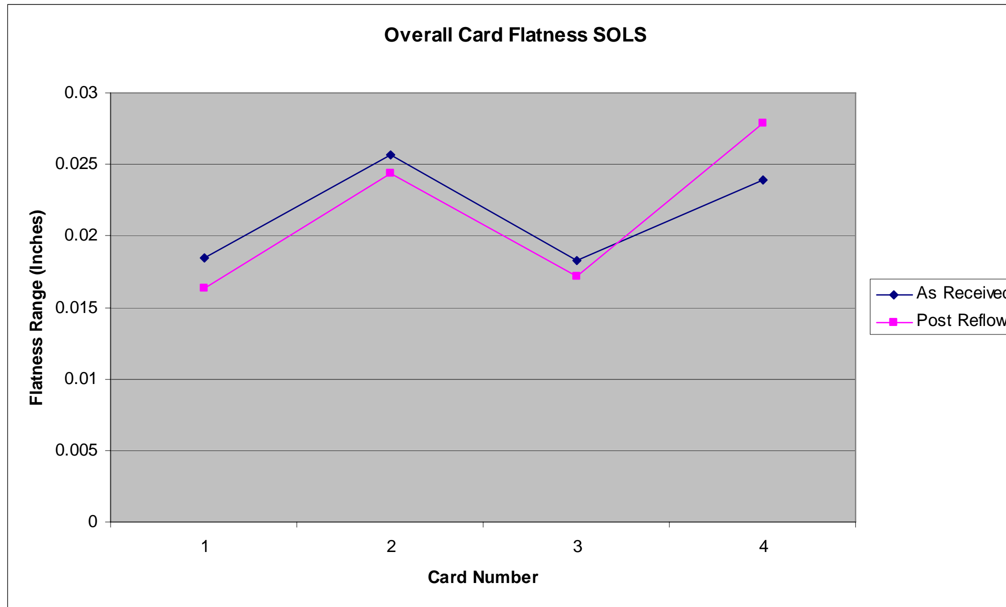
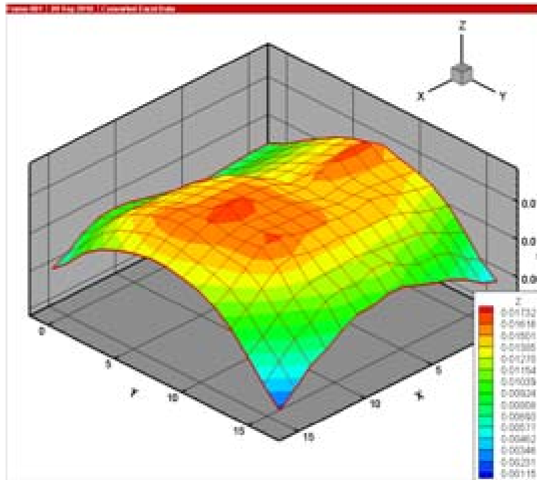
p Mid-range, 173 mil thick: Overall Card Flatness

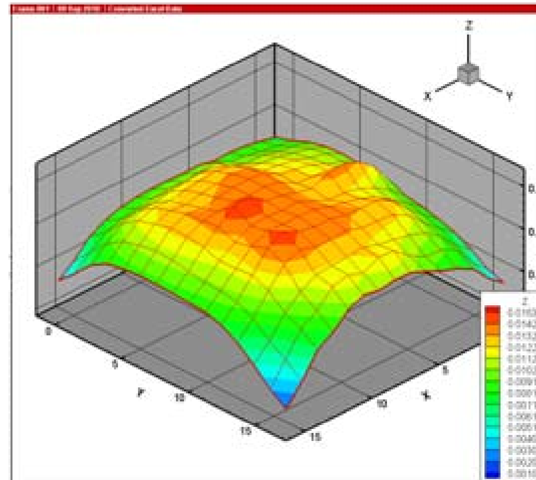


- Flatness Requirement: 0.75% max
- 16.39” x 17.14”
- 0.123” max x 0.129” max

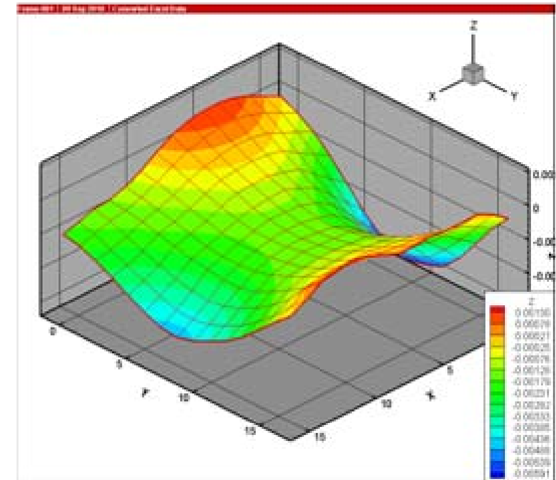
CD 1: As Received Overall Flatness



CD 1: Post Reflow Overall Flatness



CD 1: Delta Overall Flatness



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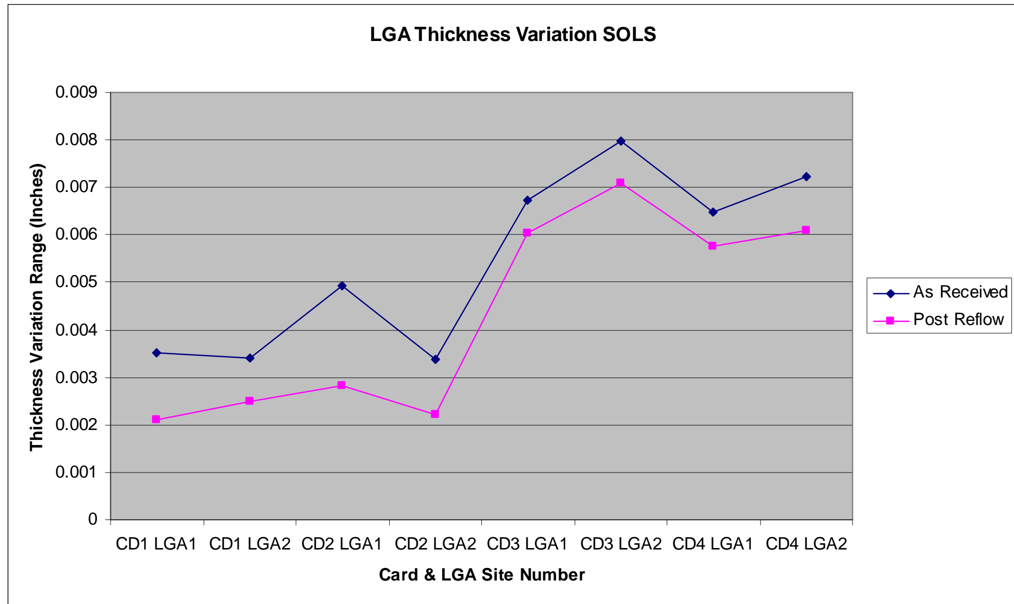
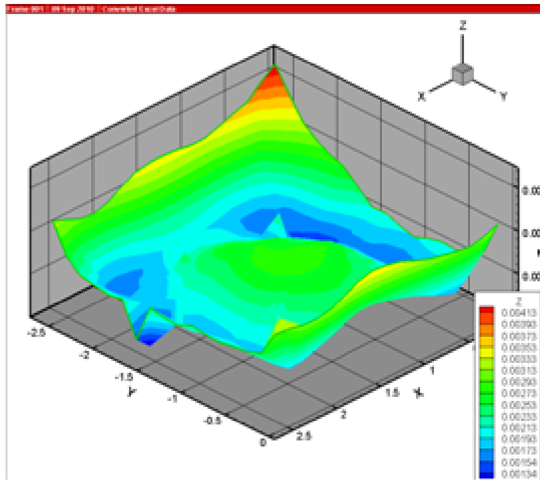
p Mid-range, 173 mil thick: LGA Thickness Variation

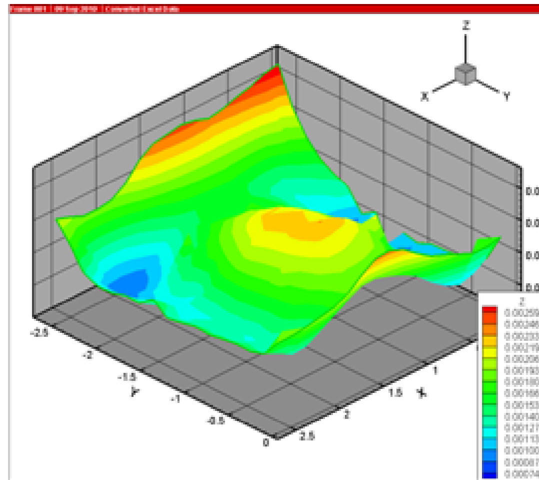


- Thickness Variation Requirement: 0.000 to 0.005 inch

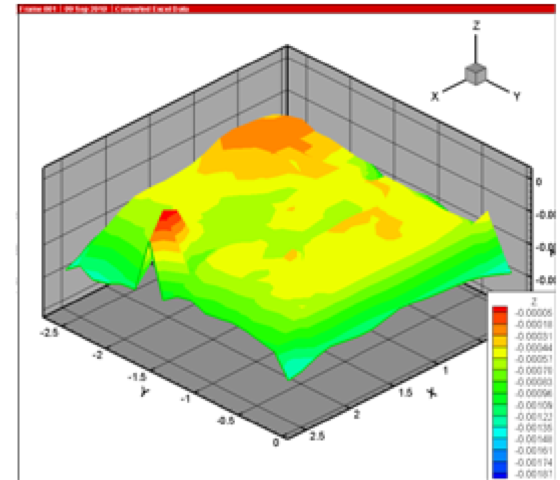
CD 2 LGA1: As Received LGA Thickness Variation



CD 2 LGA1: Post Reflow LGA Thickness Variation



CD 2 LGA1: Delta LGA Thickness Variation



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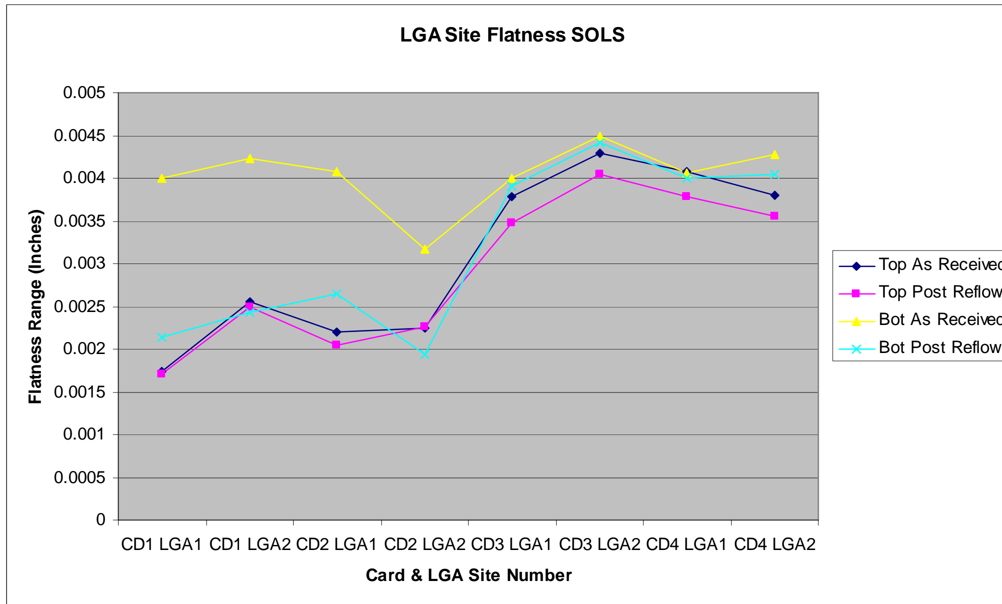
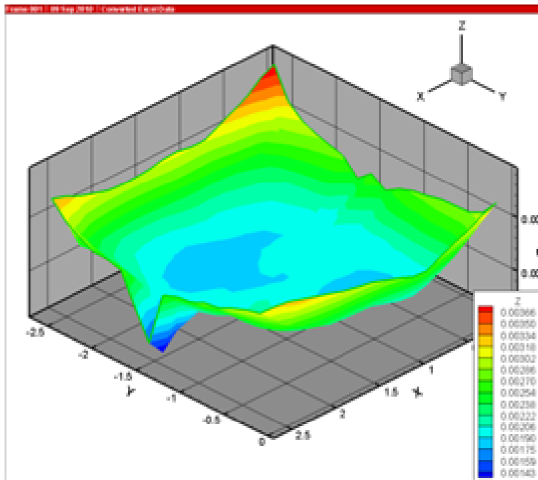
p Mid-range, 173 mil thick: LGA Flatness

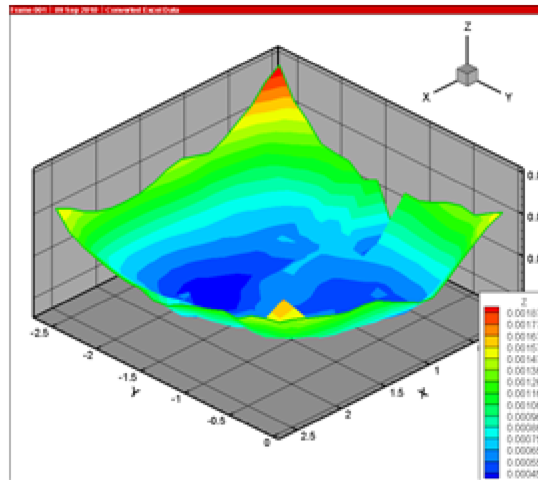


- No LGA Flatness Requirement

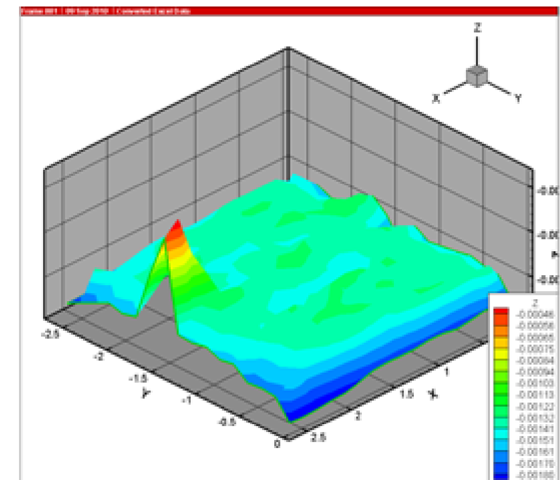
CD 1 LGA 1 : As Received Bottom Flatness



CD 1 LGA 1: Post Reflow Bottom Flatness



CD 1 LGA 1: Delta Bottom Flatness



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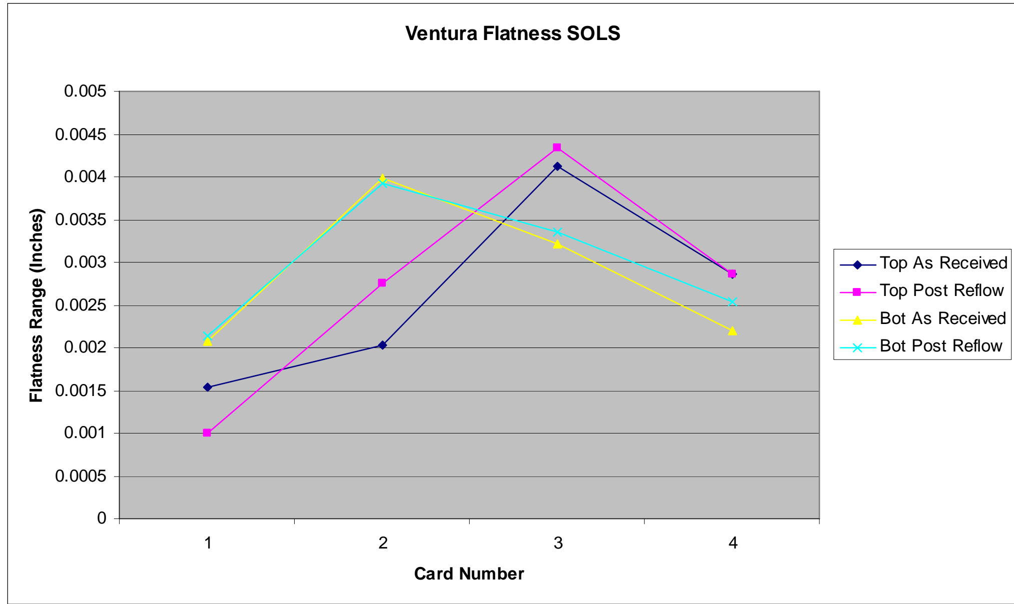
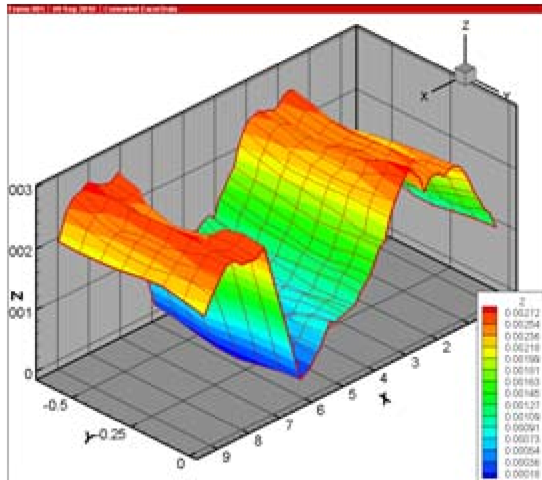
p Mid-range, 173 mil thick: SMT Connector Flatness

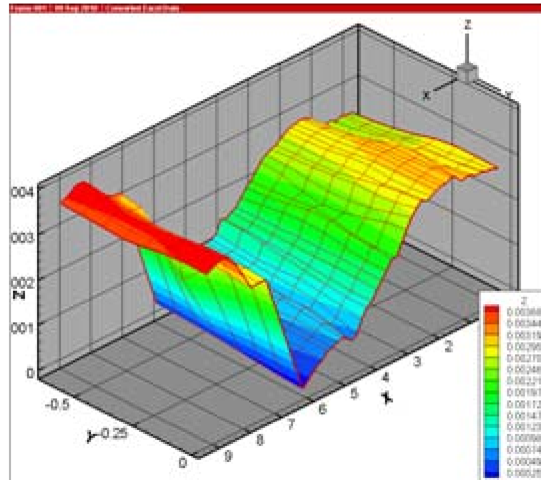


- Flatness Requirement: 5 mils / inch
- 8 x 70 = 6.2 inches
- Power = 1.9 inches

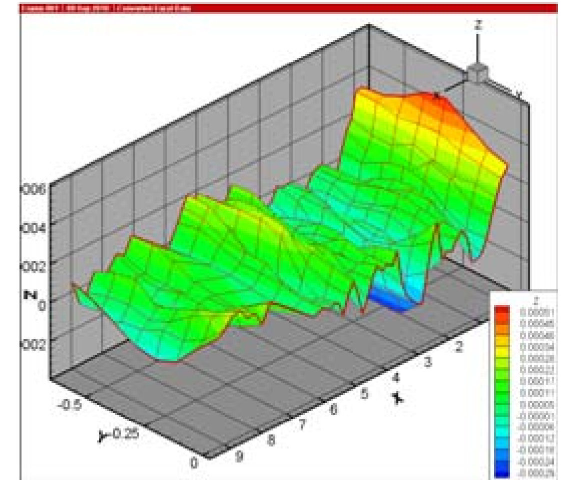
CD 2: As Received Bottom Ventura Flatness



CD 2: Post Reflow Bottom Ventura Flatness



CD 2: Delta Bottom Ventura Flatness



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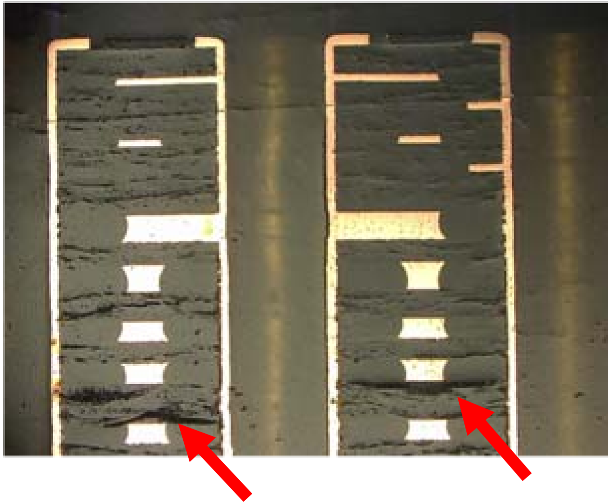
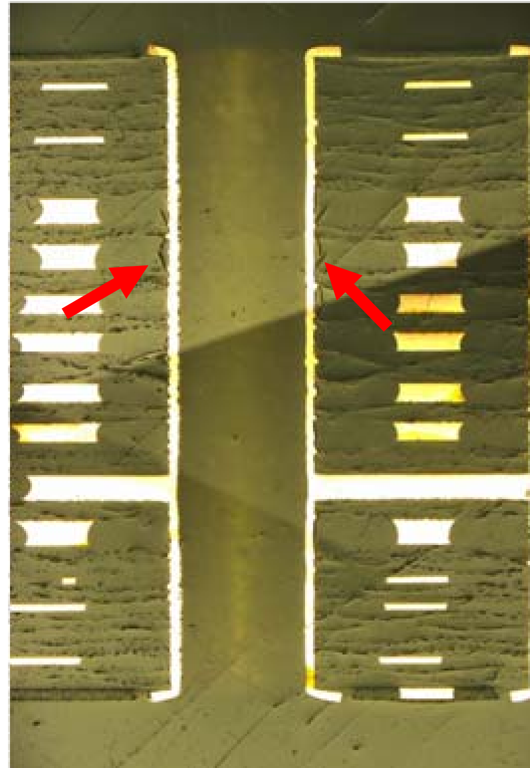
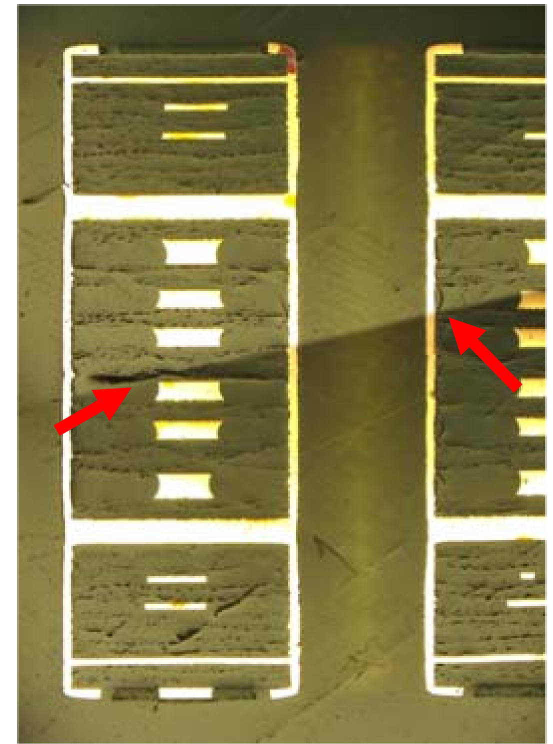
I/O Drawer, 135 mil, 4 oz. Cu

Note: Non-lead-free compatible material







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z HE PCB Qualification Strategy

- **z HE PCB presents unmatched challenges in lead-free qualification**
  - Very thick ~250 mils
  - High reflow temperature exposures with extended dwell times
- **Feasibility study using worst case global profiles**
  - 2X 245C + 2X 260C in convection
  - Mixed results, depending on construction some delamination observed (LGA site)
- **T0 testing revised preconditioning – LVP reflow attach of 14 row connector**
  - 2X 245C convection + LVP
  - PCB results passed
- **T1 testing revised preconditioning - added site rework exposures**
  - 2X 245C convection + 5X LVP (14 row connector) + 2X Hot Gas (14 row connector) + 6X Hot Gas (8 row connector)
  - PCB results good to date

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Lead-free Compatible Surface Finishes

- **Surface finish selection must balance:**
  - Assembly process challenges
  - Longer term hardware reliability performance
  - Representative environment operating conditions

	Benefits	Drawbacks / Risks	IBM
OSP HT	▪ Proven reliability ▪ Harsh environment performance ▪ High incoming quality	▪ Small assembly process windows ▪ Handling and storage ▪ PTH hole fill issues ▪ Test pin probability	✓
Immersion Silver	▪ Similar thermal fatigue reliability to OSP ▪ Improved pad wetting & PTH barrel fill	▪ Incoming quality control ▪ Harsh environment corrosion risks	X
Lead-free HASL	▪ Test pin probability ▪ Improved pad wetting & PTH barrel fill ▪ Larger process windows reported ▪ Corrosion resistance improvements	▪ Potential PCB damage HASL process ▪ Unknown high reliability performance ▪ Minimal industry data ▪ Supply quality concerns	X
Immersion Tin	▪ Corrosion resistance improvements	▪ Minimal industry data ▪ Process window limitations ▪ PTH copper dissolution ▪ Tin whisker risk	? **(OEM)**

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Summary

- Lead-Free PCB Temperature Compatibility Summary
  - Significant progress in the transition to lead-free soldering
    - First IBM systems introduced in 2009
    - New IBM systems across the portfolio by 2012
  - PCB capability critical to extending lead-free soldering introduction
    - PCB qualification simulated assembly exposures not designed to replicate exact assembly thermal process
    - Simulates the cumulative thermal stress of actual exposures
    - Simplified protocol enables preconditioning capability at more locations
  - Significant qualifications complete for 245 °C and 260 °C reflow
    - Majority are standard loss laminates
    - Lead-free soldering is now BAU for IBM products
  - Progress made on mid-loss & low loss technology qualifications
  - HE PCB qualifications remain a significant hurdle for 2012
  - Surface finish
    - OSP remains only fully qualified surface finish for IBM products
    - OEM hardware brings other finishes, immersion tin new to evaluations

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Back-up

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Example of option #4 thermal exposure simulation process flow

1. HHH @ 245'C__________: Program Name: Magnum Lead free Bot (All) ;
Use Reflow frame > Magnum bottom side fixture with the 8 rows going in first.

2. HHH @ 245'C 1X____ Program Name: Magnum Lead Free fixtureless No J1 Top (All).
Use Reflow frame > Magnum Top side EUH fixture.(8 rows going in first).

3. Please review the next 7 LVP simulation steps for J1 14R ventura
    SIMULATE ONLY > USE A DUMMY 14R VENTURA CONNECTOR FOR THERMAL MASS FOR EACH ATTACH & REMOVE STEP
    SIMULATE ONLY > NO SOLDER WILL BE APPLIED FOR J1 SEQUENCE

__________ J1 14R ventura using the LVP attach method > simulate only = Initial attach
__________ J1 14R ventura removal reflow in LVP > simulate only = 1X rework remove
__________ J1 14R site dress in hot gas tool > simulate only = 1X rework site-dress
__________ J1 14R ventura attach reflow in LVP = 1X rework attach
__________ J1 14R ventura removal reflow in LVP > simulate only = 2X rework remove
__________ J1 14R site dress in hot gas tool > simulate only = 2X rework site-dress
__________ J1 14R ventura attach reflow in LVP = 2X rework attach

4. Please review the next 6 LVP simulation steps for 8R ventura
    SIMULATE ONLY > USE A DUMMY 8R VENTURA CONNECTOR FOR THERMAL MASS FOR EACH ATTACH & REMOVE STEP
    SIMULATE ONLY > NO SOLDER WILL BE APPLIED FOR 8ROW SEQUENCE
    SPECIFIC 8ROW REWORK SIMMULATION REQUIRMENTS (i.e add 8rows connector for thermal mass)

__________ JGX06 8Row ventura attach in Hot gas tool > simulate only = Initial attach
__________ JGX06 8Row ventura removal flow in Hotgas Tool > simulate only = 1X rework remove
__________ JGX06 8Row ventura site dress in hot gas tool > simulate only = 1X rework site-dress
__________ JGX06 8Row ventura attach in > simulate only = = 1X rework attach
__________ JGX06 8Row ventura removal flow in Hotgas Tool > simulate only = 2X rework remove
__________ JGX06 8Row ventura site dress in hot gas tool > simulate only = 2X rework site-dress
__________ JGX06 8Row ventura attach in > simulate only = 2X rework attach

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