Coreless Substrate and its Extension
Performance and Future Direction

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Coreless substrate has been developed since 2001, and started HVM from 2007.
Strong demand increase is expected.
It is booming, now.

<NOTE>
- Data: as of 5/31/ 2012
- SHINKO Fiscal Year : 4/1 - 3/31
Small and Large

70mm x 70mm
17mm x 17mm

7 Layers
0.35mm thickness

9 Layers
0.41mm thickness
Warpage control

Warpage control is key to use coreless.

- at room temperature
- during die assembly process
- after die assembly

Cored Substrate Warpage
BGA: 45mm x 45mm

Coreless Substrate Warpage
Warpage control

Cause

✓ Non-uniform mechanical properties among layers
✓ Lower mechanical strength due to coreless

Solution approach

✓ Insulation resin: CTE & Y.M., close to Cu
✓ Solder resist: CTE & Y.M., close to unsulation resin’s
✓ Strengthen layer: Low CTE and high Y,M resin
Warpage at Room Temperature

Effect from Lower CTE and Higher Y.M.

<table>
<thead>
<tr>
<th></th>
<th>Original</th>
<th>1</th>
<th>2</th>
</tr>
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<tbody>
<tr>
<td><strong>Insulation resin</strong></td>
<td></td>
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<tr>
<td>CTE (ppm)</td>
<td>46</td>
<td>23</td>
<td>23</td>
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<tr>
<td>Y.M. (GPa)</td>
<td>4.0</td>
<td>7.5</td>
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<tr>
<td><strong>Solder resist</strong></td>
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<tr>
<td>CTE (ppm)</td>
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<td>40</td>
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<tr>
<td>Y.M. (GPa)</td>
<td>2.5</td>
<td>2.5</td>
<td>4.0</td>
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</table>

**Warpage (concave from die side)**

- <= 0
- <= 25
- <= 50
- <= 75
- <= 100
- <= 125
- > 125

223 um  114 um  102 um
## Warpage at Room Temperature

### Effect of Strength Layer

<table>
<thead>
<tr>
<th></th>
<th>2</th>
<th>3</th>
</tr>
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<td>Insulation resin</td>
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<td>CTE (ppm)</td>
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</tr>
<tr>
<td>Y.M. (GPa)</td>
<td>7.5</td>
<td>7.5</td>
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<tr>
<td>Strength Layer</td>
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<td></td>
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<tr>
<td>CTE (ppm)</td>
<td>N.A.</td>
<td>17</td>
</tr>
<tr>
<td>Y.M. (GPa)</td>
<td>N.A.</td>
<td>16.5</td>
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<tr>
<td>Warpage (concave from die side)</td>
<td><img src="image1" alt="Image" /></td>
<td><img src="image2" alt="Image" /></td>
</tr>
</tbody>
</table>

- Blue: <= 0
- Blue: <= 25
- Blue: <= 50
- Light blue: <= 75
- Light red: <= 100
- Red: <= 125
- Dark red: > 125

102 um 70 um
Warpage during Die assembly

Warpage change with temperature transition

Higher CTE

Lower CTE

Concave

Convex

Chip area warpage (um)

Temperature (C)

0  50  100  150  200  250

-100  -50  0  50  100
## Warpage During Die Assembly

Warpage at Die Assembly temperature can be also reduced by material combination.

<table>
<thead>
<tr>
<th></th>
<th>Original</th>
<th>1</th>
<th>4</th>
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<tr>
<td><strong>Room Temp</strong></td>
<td><img src="223um.png" alt="Image" /></td>
<td><img src="115um.png" alt="Image" /></td>
<td><img src="67um.png" alt="Image" /></td>
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<tr>
<td><strong>Temp. depend.</strong></td>
<td>223um</td>
<td>115um</td>
<td>67um</td>
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<td>(die area warp.)</td>
<td><img src="chart1.png" alt="Graph" /></td>
<td><img src="chart2.png" alt="Graph" /></td>
<td><img src="chart3.png" alt="Graph" /></td>
</tr>
</tbody>
</table>
Warpage after Die Assembly

Under fill resin causes another warpage

W/O Under fill: 86um warp.

With Under fill A: 658 um warp.

With Under fill B: 444 um warp.
Warpage after UF cured

- Any type of under fill causes warpage after cure
- Larger die area warpage = Larger BGA warpage

Diagram:

- Location-X [mm] vs. Warpage [mm]
- BGA: 55mm x 55mm

Legend:
- W/O UF
- A
- C
- D
- E
- B

Graph showing warpage and location-X for various conditions.
Under fill causes Die Area Warpage

Outside of Die Area is straight, and deformed tangentially resulting in ball co-planarity issues in the case of Large size BGA

BGA: 55mm x 55mm
Stiffener for Warpage Control

Structure

- Die
- Stiffener
- BGA Substrate

Cross section

With stiffener

- Stiffener
- Die
- BGA Substrate

W/O stiffener

- Die
- BGA Substrate
Stiffener Effect / Simulation (25 deg.C)

Bare substrate

Unit area warpage: 
-446 um
Die area warpage: 
-88 um

Stiffener attached

38 um
9 um

Die assembled with Underfill

399 um
192 um

Die assembled with Underfill

193 um
178 um

Deformation scale x10
Stiffener Effect / Measurement (25 deg.C)

Warpage before Die Assembly

Warpage after Die Assembly

✅ Stiffener improves the BGA Warpage caused by Underfill
Insertion & Reflection Loss

Coreless substrate = Small insertion loss
Electrical Characteristics

Signal Integrity

Core Substrate = 10 Ω lower Zdiff than Coreless
Loop L simulation

0.4mm core

0.1mm core

coreless

Package Model
Layer proximity effect

Short length effect

**Thinner core and coreless enable reduced Loop L**

![Graph showing Loop L values for different power sources and core configurations at 100MHz.](image)

- **Power Integrity**

Electrical Characteristics

- Thinner core and coreless enable reduced Loop L

![Diagram](image)

- @100MHz
Electrical Characteristics  Power Integrity

Droop simulation
800um core

Coreless

2/4/2 structure
7+1 layer structure

Port1 (FC side)
VDD
VSS

Port2 (BGA side)
VDD
VSS
Coreless enables improved 1st droop (10% better) due to lower inductance.
Extension of Coreless Substrate

- "Silicon interposer"
- "Organic interposer" extension for cost sensitive area
- Build up substrate

Level/Sketch (um):
- 2D: 10/10
- 2.5D: 8/8
- 3D: 5/5
- 2.5D: 3/3
- 2.5D: 2/2
- 2.5D: 1/1
- 2.5D: <1/1

Layers:
- Silicone interposer
- Organic interposer
- Organic substrate
Coreless manufacturing process has advantages for higher density routing.

- It is built on Cu plate, not on CCL
- Stable through heating process
- Flat surface
- Smaller via pad diameter
- Finer photo resist patterning
- Opportunities of resin selection
Extension of Coreless Substrate

◆ Examples of fine L/S patterning  (L/S=8um/8um)

After resist development

After seed layer etching

✓ L/S<10/10um can be fabricated with conventional SAP technology
Examples of fine L/S patterning (L/S=5um/5um)

After resist development:
- DFR
- Seed layer

After seed layer etching:
- Resin
- Cu

L/S=5/5um was successfully demonstrated over smooth resin surface
Summary:

- Demonstrated that conventional SAP technology could be extended beyond L/S=10um/10um
- Applicable to high density interposer for 2.5D Interconnection

Concept of high density interposer for 2.5D
Summary

Warpage control

Balanced effective properties among layers

- Lower CTE & Higher Y.M. resin
- Mixed material selection among layers according to design
- Solder resist material selection

Strengthen layers

Stiffener combination for large size BGA
Summary

Electrical Characteristics

- Coreless Signal and Power integrity are better than current PKG, due to good Z0 matching around Via and Lower Loop inductance

Extension of coreless substrate

- Demonstrated that conventional SAP technology could be extended beyond L/S=10um/10um. It’s applicable to high density interposer for 2.5D Interconnection
Thank you very much