The Past....
• The need for more efficiency in all walks of life is kick started....

• This includes the electronics industry and the continual drive to smaller, higher performance, and greatly improved efficiency

• Power Supplies are a logical focal point for energy efficiency improvement
Linear Power Supply – Poor Efficiency (Large Heatsink Required)
Schematic Generation – Old School... Early SMPS
Development of HEXFET – SMPS Break Through….

1947: Founded in Los Angeles
1962: Developed industry’s first epitaxial process
1983: Developed one of the first intelligent power ICs
1993: World’s first SmartFET
1999: World’s highest density and lowest RDS(on) MOSFETs
2001: iPOWER building blocks for DC-DC
2003: iMOTION platform for variable speed motor drivers
1959: Developed first silicon-controlled rectifier
1979: Developed the HEXFET™
1983: First patents for power MOSFETs and IGBTs
1996: World’s first FETKY™ product
2000: FlipFET™ wafer-level packaging
2002: DirectFET™ packaging technology breakthrough
2008: Introduced industry leading GaN technology

1979: Developed the HEXFET™
Early Switching Power supplies for DC-DC
The Present....
Typical Single Phase DC-DC Switching Power Supply

Controller + Drivers

FETs
Discrete FETs – Packaging Advancements Reduce Size

**Improve Power Density with Dual Cool™ Packaged MOSFETs**

- More than 60% better power dissipation
- Highest power density for DC-DC applications
- Lower operating temperature increases reliability

**Cool power**

- Thermal performance comparison

**Dual MOSFETs LCC-6**

**DUAL MOSFETS**

- CMLDM7003 (USA Pinout)
- CMLDM7003J (Japanese Pinout)

**QFN 5x6**

- 8 x 21
- 168mm²

- 1.5mm spacing between components and boundaries

- 14.5 x 17.5
- 254mm²
Integrated Power Stage– Driver + FETs

Figure 1: Driver plus FET Multi-Chip Module (DrMOS)
Point Of Load (POL) Design Simplicity and Size Reduction

6.8V < Vin < 16V

Board area: ~100 mm²
Board area: 30 mm²

70% size reduction compared to discrete solution with 2 x SO8 FETs
35% size reduction compared to discrete solution with a Dual SO8 FET
POL Devices Evolving into Smaller and Higher Current Products

<table>
<thead>
<tr>
<th>3.3V or 5V bias</th>
<th>Ultra-Efficient at light load</th>
<th>12Vin Self-Biased</th>
<th>3.3V bias/input</th>
<th>12Vin Self-Biased</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.7x7.7mm</td>
<td>4x5mm</td>
<td>4x5mm</td>
<td>3x3mm</td>
<td>5x6mm</td>
</tr>
<tr>
<td>IP1837</td>
<td>IR3863</td>
<td>IR3897</td>
<td>IR3884</td>
<td>IR3894</td>
</tr>
<tr>
<td>IP1827</td>
<td>IR3865</td>
<td>IR3898</td>
<td>IR3886</td>
<td>IR3895</td>
</tr>
<tr>
<td>25A, 35A</td>
<td>6A, 10A</td>
<td>3A, 6A, 9A</td>
<td>4A, 6A</td>
<td>10A, 16A</td>
</tr>
</tbody>
</table>
Early Wire Bond Integrated POL Device

* Packaging Technology is a big part in driving product integration…
Integrated POL Modules

9A DC-DC Converter Module - +12Vin to +0.7 – +5.0 Vo

15A Module in a 15 x 15mm package
The Future....
GaN – Power Device Technology Platform

• Traditional Si based FETs have reached their peak FOM
• Gallium Nitride based Transistors set new Standards for FOM
• Allows for much higher frequency, denser designs w. very good efficiencies
• Low Cost and Reliable production methods using GaN-on-Si Hetero-epitaxy - Device manufacturing process is CMOS compatible
• Standard high volume production has started
FOM Requirement for Efficient and Dense Conversion

Ron*Qg FOM (mOhm*nC) vs. Switching Frequency (MHz)

- 30 V Si Limit
- 30 V GaN Target
- 30 V GaN Limit

88% efficiency
12Vin, 1.2Vout, 25A

Simulation
0 5 10 15 20 25 30

Ron*Qg FOM (mOhm*nC)
0 1 10 100 1000

Add another slide from Mike's presentation
Flagship High Frequency LV DC-DC performance

High Frequency GaN Power Stage Efficiency

- Today: 5 MHz, Vout = 1.8V
- Today: 10 MHz, Vout = 1.8V
- 2 Years ago: 5 MHz, Vout = 1.8V
Size Matters… GaN based solution footprint reduction

Increasing Frequency : Significant Footprint Reduction

300 kHz

300kHz 2-Phase
Height 4-5mm
1530mm²

1 MHz

1MHz 2-Phase
Height 3mm
540mm²

3x PCB reduction
Current GaN Based POL Device 6x6 mm

Vin=12V, Vout=1.2V, fsw=1.2MHz

Efficiency

Current (A)
GaN Power Stage Roadmap

* Size and Efficiency Improvements for a 100A, 12V – 1.2V Multi-phase DC-DC Converter
Frequency Requirements for Dense Power Conversion

* Higher Power Densities leading towards direct Vcore Power Generation from the Processor Logic with cavity filled power delivery...

![Graph showing Buck Converter Switching Frequency (MHz) vs Conversion Current Density (A/cm²). The data indicates a range of 100 to 300 A in 200 to 300 mm² (CPU die) = 30 to 150 A/cm².](image)
Processor Core Power (Integrated Power Stages)

Why? – Smaller size, lower cost, lower power impedance, less losses, simplified layout ….
Processor Core Array
Increased Power Densities – New Product Evolution
Increased Power Densities – New Product Evolution (Cont.)
Increased Power Densities – New Product Evolution (Cont.)
Increased Power Densities – New Product Evolution (Cont.)