Digital Power Management:

A requirement....

Not an option

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System Power Management

12 volt Bus

System Management

System Supervisor

Local Control Bus

1.1V

3.3V

1.35V

1.5V

Multiphase VRD

Chip 1

Chip 2

Memory

Memory

Memory

Memory

Processor

Digital Systems Tomorrow
Digital power management is required

Key areas of

Digital Power Management advancement

- Introduction
- Diagnostics and communication
- Efficiency and loss management
- Transient response
Power Management Communication

- Communication is digital throughout the infrastructure
  - Digital communication with power IC is expected
  - Bus has bi-directional communication
  - Bus tends to be proprietary per end silicon at load ASIC

- Digital communication to the system environment from power IC
  - Open bus structure available; PMBus, I2C etc
  - Telemetry information: Voltage, temperature, current power, average current over long time blocks
  - Fault information
  - Typically a lower frequency I2C bus at 100Khz to 400Khz

- Digital Communication between silicon load and power IC device
  - Power functions are defined on the serial bus
  - Optimization of efficiency and power consumption can be accomplished across all runtime scenarios of various architectures
  - High frequency bus operable >20 MHz
Simplified Control Block

Digital control IC

- S/H
- VADC
- PID (Compensator)
- DPWM
- VID sense
- Isum & AVP Filter
- IADC
- State machine

Digital Output

- FET Driver
- Digital Output

Analog sense

- Analog sense
- Analog sense

System

- Serial Bus
- High speed serial bus

Load
Key areas of Digital Power Management advancement

- Introduction
- Diagnostics and communication
- Efficiency and loss management
- Transient response
Diagnostics and Communication

- Full communication of key telemetry parameters of power solution to the System
  - Temperature of devices
    - IC temperature data
    - FET temperatures
  - Voltage and current telemetry
  - Characterization of loads can easily be accomplished
    - Blocks of average current - seconds of time
    - Peak currents of load data can be characterized
  - Power data can be streamed to the system or ASIC
  - Fault reporting

- System response to the stream of data. What do you do with it?
  - Intelligently use the data for system optimization and function
  - Respond to the data for making decisions to turn on and off power
  - Early warning of parameters exceeding operating characteristics
Fault communication and diagnostics

- **Fault communication**
  - Faults can be reported to system
    - OCP, OVP, UVP, VinUVP, VinOVP, temperature, duty-cycle
  - Fault and key data information can be streamed to system or load
    - Proactive response to data- Power loss, voltage, temperature.
    - Response to faults can be intelligently executed upon
    - Predicting failures before they occur

- **Black Box information**
  - Last picture of power delivery when fault occurs
    - Vin goes down
    - When a fault occurs in the circuitry of a POL rail
  - Clear picture of the failing parameter in power stage
    - Vin goes down- Status of rail reported
    - When major fault occurs- last mirror image saved for system analysis
    - Failure mode is reported
Digital power management is required

Key areas of

Digital Power Management advancement

- Introduction
- Diagnostics and communication
- **Efficiency and loss management**
- Transient response
Optimal Efficiency over load

- Digital is enabling the system to manage the consumption of power
  - Phase dropping and adding can create an approximate constant peak efficiency over loading with multiphase circuits.
  - Phasing can be dropped back to a low power state where one phase can support the ASIC voltage and current in an idle state.
  - Number of operational phases can be defined load current
    - Phase drop/add can be determined by current level in application
    - Example: Memory of 8 DIMM memory. Use 4,3,2 phases where phasing can be defined for optimal efficiency for the memory
  - Phase/gain can be programmed for each state in order to keep constant bandwidth from 1 phase to full phase operation of power stage
  - Transient response can be optimized digitally with phase changes by activating phases on transient events.
Dynamic Phasing-iPS for Memory-1.5Volt

Vout=1.5 volts
iPS-PX4650
Fo=350Khz
Dynamic Phasing-Discretes for Memory-1.5V

Low Side- BSC020N03
High Side- BSC080N03
Vout = 1.5 volts
F0 = 400Khz
2 Phase change to 4 phases
Digital power management is required

Key areas of

Digital Power Management advancement

- Introduction
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- Transient response
Transient capability improvement

- Improvement to transient response via custom algorithms
  - Non-linear/custom algorithms can run in parallel with main loop
  - Ex. Asynchronous phase firing improves transients significantly
    - Extra Pulses can be fired within 50 nSec of transient detection
  - Transient response function can occur past the bandwidth of the power stage crossover frequency.

![Diagram](image-url)

- **Vout**
- **Switch Node**
- **One phase**

100nSec
Example of 2 phase to 4 phase dynamic transient

* 10 to 60 amp transient—Meets Intel requirements

2 phase to 4 phase transition

\( V_{sw1} \)

\( V_{sw2} \)

\( V_{sw3} \)

\( V_{sw4} \)

\( R1: I_{out} \)

\( R2: V_{out} \)

\( F_o = 615 \text{Khz} \)

* 10 to 60 amp transient—Meets Intel requirements

2 phase to 4 phase transition
Improved Transient Response

Assumptions

- Load lines can be as low as .5mOhms to 1.25 mOhms for high current processors.

- If .8 mOhm load line then loop gain keeps output impedance at .8 mOhm until near the crossover frequency

- Past the bandwidth of the amplifier, the impedance of the capacitor bank determines transient response

- Digital ATR2 asynchronously adds pulses to phases when transient events take the output voltage out of regulation.

- Result- Reduced output impedance past the bandwidth of PID loop.

- Result- Reduced cost of capacitor bank components
Output Impedance testing

Digital Controller

Vin

S/H

VADC

PID (Compensator)

VIDs

FET Driver

State machine

DAC

Isum & AVP Filter

VIDs

sense amp S/H

Serial Bus

System

Bandwidth - 150kHz

Frequency VRD - 600KHz

4/5 phase operation

90A constant step load

One Phase Of Multiphase Power Stage
Output impedance of power stage

- 1024uF MLCC + 470uF Poscap - No ATR2
- 1024uF MLCC + 3x470uF Poscap - No ATR2
- 1024uF MLCC + 470uF Poscap - ATR2
- 1024uF MLCC + 3x470uF Poscap - ATR2
- 540uF MLCC - No ATR2

Legend:
- 4ph, ATRH1+3, 1pos
- 4ph, no ATR, 1pos
- ZLL_Max
- ZLL_Min
- 5ph, ATRH1+3, 3 pos
- 5ph, no ATR, 3 pos
- 4ph, no ATR, 540uF
Going Forward-
More digital advancement to come

- Advance signal warning from ASIC Load to power management devices
  - Today all control chips respond to current step event that has already occurred..... Delayed reaction
  - Can information in ASIC be characterized for load steps with advance communication of step loads and unloads in the system?
  - High speed bus can set the stage for faster communication of loads to control circuits for advancing response to loading in ASIC circuits.

- Intelligent communication between Power management and load
  - Control of voltage and current delivery to processor/ASIC load
  - Characterize load and power management in terms of voltage and current control
Summary

- Digital communication from power management control devices to the system and load infrastructure is required.
- Diagnostics, telemetry, fault information, predictive failure management, and black box info are in process of use at various stages.
- Digital algorithms for control and transient response are improving overall loss management in all current and voltage dynamics for the processor/ASIC loads.
- More control will be seen between the processor/ASIC loads and the power management devices to control voltage and current through all the various runtime events that occur in the silicon architectures going forward.