Avoiding the Pitfalls of Redundant Power Systems Design

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N+1 Power System Availability

- Power Supply 200K Hr MTBF
- Load
- PS #1
- PS #2
- Nonredundant power system
- Redundant power system w/ quarterly scheduled service
- Hot swap redundant power system; 48hr replacement

Outages/10K servers with 5 year life

1812
19.5
0.4

If only it were true...
Single Points of Failure

System Outage Probability =
  Probability of 2 failed power supplies in the system
+ Probability of all single fails that can cause a system outage

The design of a high availability power systems needs to focus on the reduction of critical failures more than the increase of power supply reliability.
Where Single Points of Failure Can Occur

- Dual Power Cords
- Redundant DC buses
- Group converter parameters
- Faulty sensors
- Faulty service action
Shorted Output Sections

Shorted output FET or Cap will bring down output bus

Addition of ORing FET (rectifier)

Rectifier – Simple but lossy
FET – Need control circuit; more efficient
Latent Failures

Undetected failures can compromise redundancy

When this fails we need to know it
...and report it to the service system

The addition of the “+1” supply is simple, but the implications are not
Separation of Regulation and Protection Circuits

Regulation and protection share remote sense amp
Regulation reference also shared

Second remote sense amp
Second reference
Second pair of sense leads

Open sense lead latent fail omitted
Regulator to Load Impedance (Penalty of Hot Plug)

Large signal approximation

\[ \Delta V_o = \frac{\Delta I^2 L}{2 (V_{\text{bulk}} - V_o) C_L} \]

L = Total L from bulk to load = \( L_p/N + L_d \)

Numerical example:

\( \Delta I = 140; \ L_p = 200\text{nH}; \ L_d = 150\text{nH}; \ N = 15; \ V_{\text{bulk}} = 12; \ V_o = 2 \)

For \( \Delta V = 20\text{mV}; \ C_L = 4000\text{uF} \)

If this were a VRM on the board (\( L_d \sim 3\text{nH} \)) \( C_L = 400\text{uF} \)

The decision to add hot plug should not be taken lightly. It may have significant impact on cost and packaging.
Overvoltage Discrimination

Bus OV does not indicate which regulator caused OV

Simple Solution

Better Yet

Duty Cycle must go to 0 to use this
Featurable Loads

Most I/O (PCI cards, Disks) and memory tend to be highly featurable

To assure N+1 redundancy, accurate current sharing & sensing required

1% current sharing with 1% current measurement accuracy is marginal here

Periodic Vout adjust up/down by service system will help
Faulty Sensor (Group Overcurrent)

Reported Currents

I=33
- PS #1: 1.1V@50A
- PS #2: 1.1V@50A

I=33
- PS #3: 1.1V@50A

I=60
- Load =100A

Defective current sensor likely

Total output current must be observed to prevent/minimize smoke during load faults

A real group overcurrent will still have balanced regulator output currents

This group does not need to be shut down, only PS#3
Input Faults

Selective coordination can be nontrivial

Similar technology circuit protection used in the PS and branch protector will generally not coordinate.

Applies to distributed DC busses also

Shorted input on VRM input can bring down both busses

Solid state protection circuits practical
Design Practices That Can Help

- FMEA analysis at system level
- Testing with real hardware
- Service modeling by service personnel
- Design reviews of microcode

“Failure of Imagination”