IBM Semiconductor design methodology

ASIC: Your design challenges. Our value.

Design flow	Tasks	How we can help you
Definition	High-level architecture	• Flexible engagement models enable you to take advantage of only the services you need • Automated insertion of test structures support full scan testability to help ensure predictable results in hardware
Synthesis	Logic synthesis, physical synthesis, design planning, design-for-test	
Physical implementation	Placement, routing, clocks, optimization	• Proven success in multimillion gate designs • Noise-aware placement and wiring can help avoid noise and congestion issues before they become problems in hardware • Full slate of power-management techniques to balance power and performance goals
Checking and sign-off	Noise, power and timing closure, design checks, extraction	• Statistical timing flow facilitates fast design-change turnaround through incremental modeling • Hardware-correlated models reliably predict performance in end hardware • Dynamic and static noise analysis help ensure correct-by-construction design • At-speed structural test provides testing capability during design at product-like clock rates for more comprehensive defect screening
Chip finishing	Design-rule checking, layout versus schematic checking, GDSII creation	

A shared goal—
first pass design success

IBM and the IBM logo are trademarks of International Business Machines Corporation in the United States, or other countries, or both.
Other company, product and service names may be trademarks or service marks of others.