



# PowerXCell 8i Processor

## Highlights

- **Improves double-precision floating-point performance (approximately eight times faster)**
  - 12.8 GFLOPS per Synergistic Processor Element (SPE)
  - Over 100 GFLOPS per IBM PowerXCell™ 8i processor
- **Increases main memory capacity up to 16 GB**
- **Cell Broadband Engine™ Architecture version 1.01 compliant, with a compatible programming model**
- **Single-chip multiprocessor includes one dual-threaded Power™ Processor Element (PPE) and eight functional SPEs**
- **High-bandwidth (over 200 GBps) on-chip communication fabric**
- **Dynamic power management, including processor frequency scaling and memory and bus sleep states**
- **Real-time support throughout the architecture**
  - Cache and translation look-aside buffer (TLB) replacement policy management
  - Bandwidth control through resource allocation
- **Logical partition and hypervisor support**

## Overview

The PowerXCell 8i processor is designed for high-performance, double-precision floating-point intensive workloads that benefit from large-capacity main memory. Applications include blade servers, high-end workstations and digital signal processors. The PowerXCell 8i processor is a high FLOPS/mm<sup>2</sup> processor with industry-standard double-data-rate (DDR2) memory. It

is an enhanced implementation of the Cell Broadband Engine Architecture.

The Cell Broadband Engine Architecture is designed for distributed processing. A PPE, which includes a Power processor unit (PPU) and a Power processor subsystem (PPSS) with a level 2 (L2) cache, manages the system and distributes tasks to the SPEs. The SPEs are highly efficient single-instruction, multiple-data (SIMD) processing units optimized for computation and data movement. An SPE consists of a synergistic processor unit (SPU) and a memory flow controller (MFC).

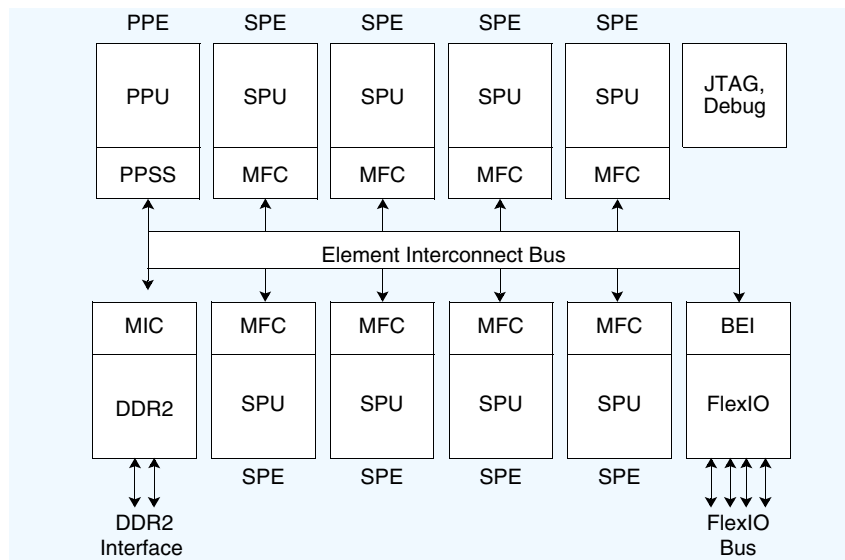
## 64-Bit Power Processor Element

- Dual-instruction issue; two threads, simultaneous multithreading (SMT)
- 32 KB instruction cache, 2-way set associative
- 32 KB data cache, 4-way set associative, write-through
- 128-byte cache line size
- 64 gigabytes per second (GBps) load-and-store bandwidth

- 512 KB 8-way set-associative, store-in L2 cache
- Multiple page size support: 4 KB and two sizes selectable from 64 KB, 1 MB or 16 MB

## Synergistic Processor Elements

- Instruction set architecture organized to support SIMD capability
- 128 128-bit registers (1 quadword, 2 doublewords, 4 single words or 8 halfwords)
- Floating-point throughput of 25.6 GFLOPS for single-precision or 12.8 GFLOPS for double-precision
- Dual issue pipeline:
  - One simple or complex fixed-point or floating-point operation
  - One load-and-store, branch, shuffle or quadword rotate operation
- 256 KB local store memory
  - 16-byte access to or from local store
  - 128-byte direct memory access (DMA) read and write



## PowerXCell 8i Processor Specifications

Technology	Complementary metal-oxide semiconductor (CMOS) silicon on insulator (SOI) 65 nm
Die size	212 square mm
Packaging	1827 leads, 47.5 × 47.5 mm plastic ball grid array (PBGA), 1 mm pitch
Signal I/Os	837
Temperature range (Tj)	5 to 90°C
Interfaces	Dual 144-bit DDR2 800 Mbps memory channels Five 8-bit FlexIO links at 5 GBps each, configurable as two FlexIO buses
Frequency (SPE and PPE)	Up to 3.2 GHz
Performance (est.)	More than 200 GFLOPS at 3.2 GHz
Power Supply	1.0 V V <sub>DD</sub> , 1.5 V V <sub>DDA</sub> , 1.8 V V <sub>DD18</sub> and 1.2 V V <sub>DDIO</sub> ±2%
Maximum power dissipation (est.)	92 W

### Memory Flow Controller (MFC)

- Programmable DMA unit
- Up to 16 simultaneous memory operations with DMA-list support
- Atomic facility for lock management

### Memory Interface Controller (MIC)

- DDR2 with two or four dual in-line memory modules (DIMMs) up to 800 MHz
- 1 GB to 32 GB (64 GB using 2 Gb dynamic random-access memory [DRAM])
- Up to 25.6 GBps bandwidth
- Optional single error correction and double error detection (SEC - DED) error checking and correction (ECC) with a 144-bit interface

### PowerXCell 8i Interface Unit (BEI)

- Five Rambus FlexIO links of 5 GBps each, configurable as two FlexIO buses
- One or two CBEA noncoherent I/O interface (IOIF) protocols, or one coherent PowerXCell 8i interface (BIF) protocol or both
- Up to 20 GBps coherent BIF dual-processor interconnect

### Peripherals

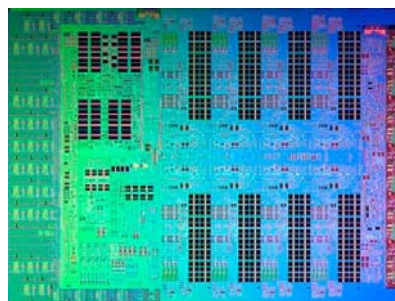
The PowerXCell 8i processor supports a full range of peripherals attached through the IBM south-bridge chip.

### Other Features

- Interrupt controller with 16 priority levels
- Institute of Electrical and Electronics Engineers (IEEE) 1149.1 Joint Test Action Group (JTAG) boundary scan support and test access port
- Serial peripheral interface (SPI) and RISCWatch support
- Logic and array built-in self tests (BISTs)
- Parity-protected instruction cache and data cache
- ECC-protected L2 cache and SPU local stores

### Development Support

The Cell Broadband Engine Architecture is supported by a complete software development kit (SDK). The SDK provides a full range of development tools, including a compiler, a debugger, an architectural simulator, performance analysis tools and sample code.



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