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IBM System z10 Business Class and Enterprise Class Overview

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IBM System z Family
IBM System z family

IBM System z9 EC (2094)
- Announced 7/05 - Superscalar Server with up to 64 PU cores
- 5 models – Up to 54-way
- Granular Offerings for up to 8 CPs
- PU (Engine) Characterization
  - CP, SAP, IFL, ICF, zAAP, zIIP
- On Demand Capabilities
  - CUoD, CIU, CBU, On/Off CoD
- Memory – up to 512 GB
- Channels
  - Four LCSSs
  - Multiple Subchannel Sets
  - MIDAW facility
  - 63.75 subchannels
  - Up to 1024 ESCON® channels
  - Up to 336 FICON channels
  - FICON Express4 and 2
  - OSA 10 GbE, GbE, 1000BASE-T
  - Coupling Links
- Configurable Crypto Express2
- Parallel Sysplex™ clustering
- HiperSockets™ – up to 16
- Up to 60 logical partitions
- Enhanced Availability
- Operating Systems
  - z/OS, z/VM, z/VSE®, TPF, z/TPF, Linux on System z

IBM System z9 BC (2096)
- Announced 4/06 - Superscalar Server with 8 PU cores
- 2 models – Up to 4-way CPs
- High levels of Granularity available
  - 73 Capacity Indicators
- PU (Engine) Characterization
  - CP, SAP, IFL, ICF, zAAP, zIIP
- On Demand Capabilities
  - CUoD, CIU, CBU, On/Off CoD
- Memory – up to 64 GB
- Channels
  - Two LCSSs
  - Multiple Subchannel Sets
  - MIDAW facility
  - 63.75 subchannels
  - Up to 420 ESCON channels
  - Up to 112 FICON channels
  - FICON Express4 and 2
  - OSA 10 GbE, GbE, 1000BASE-T
  - Coupling Links
- Configurable Crypto Express2
- Parallel Sysplex clustering
- HiperSockets – up to 16
- Up to 30 logical partitions
- Enhanced Availability
- Operating Systems
  - z/OS, z/VM, z/VSE, TPF, z/TPF, Linux on System z

IBM System z10 EC (2097)
- Announced 2/08 - Server with up to 77 PU cores
- 5 models – Up to 64-way
- Granular Offerings for up to 12 CPs
- PU (Engine) Characterization
  - CP, SAP, IFL, ICF, zAAP, zIIP
- On Demand Capabilities
  - CoD, CIU, CBU, On/Off CoD, CPE
- Memory – up to 1.5 TB for Server and up to 1 TB per LPAR
  - 16 GB Fixed HSA
- Channels
  - Four LCSSs
  - Multiple Subchannel Sets
  - MIDAW facility
  - 63.75 subchannels
  - Up to 1024 ESCON channels
  - Up to 336 FICON channels
  - FICON Express8, 4, and 2
  - OSA 10 GbE, GbE, 1000BASE-T
  - InfiniBand Coupling Links
- Configurable Crypto Express2
- Parallel Sysplex clustering
- HiperSockets – up to 16
- Up to 60 logical partitions
- Enhanced Availability
- Operating Systems
  - z/OS, z/VM, z/VSE, TPF, z/TPF, Linux on System z

IBM System z10 BC (2098)
- Announced 10/08 – Server with up to 77 PU cores
- Single model – Up to 64-way
- Granular Offerings for up to 12 CPs
- PU (Engine) Characterization
  - CP, SAP, IFL, ICF, zAAP, zIIP
- On Demand Capabilities
  - CoD, CIU, CBU, On/Off CoD, CPE
- Memory – up to 256 GB for Server
  - 8 GB Fixed HSA
- Channels
  - Two LCSSs
  - Multiple Subchannel Sets
  - MIDAW facility
  - 63.75 subchannels
  - Up to 480 ESCON channels
  - Up to 128 FICON channels
  - FICON Express8, 4, and 2
  - OSA 10 GbE, GbE, 1000BASE-T
  - InfiniBand Coupling Links
- Configurable Crypto Express2
- Parallel Sysplex clustering
- HiperSockets – up to 16
- Up to 30 logical partitions
- Enhanced Availability
- Operating Systems
  - z/OS, z/VM, z/VSE, TPF, z/TPF, Linux on System z

Currently “As Available”
Statements of Direction* as of August, 2009

- **The System z10 will be the last server to support connections to the Sysplex Timer (9037).** Servers that require time synchronization, such as to support a base or Parallel Sysplex, will require Server Time Protocol (STP). STP has been available since January 2007 and is offered on the System z10, System z9, and zSeries 990 and 890 servers.

- **The System z10 will be the last server to support Dynamic ICF expansion.** This is consistent with the Statement of Direction in Hardware Announcement 107-190, (RFA44930) dated April 18, 2007: "IBM intends to remove the Dynamic ICF expansion function from future System z servers."

- **ICB-4 links to be phased out.** IBM intends to not offer Integrated Cluster Bus-4 (ICB-4) links on future servers. IBM intends for System z10 to be the last server to support ICB-4 links as originally stated in Hardware Announcement 108-154, dated February 26, 2008.

- **ESCON channels to be phased out.** It is IBM's intent for ESCON channels to be phased out. System z10 EC and System z10 BC will be the last server to support greater than 240 ESCON channels.

- **IBM intends to support optional water cooling on future high-end System z servers.** This cooling technology will tap into building chilled water that typically exists within the datacenter for computer room air conditioning systems. External chillers or special water conditioning will typically not be required. Water cooling technology for high-end System z servers will be designed to deliver improved energy efficiencies.

- **IBM intends to support the ability to operate from High Voltage DC power on future System z servers.** This will be in addition to the wide range of AC power already supported. A direct HV DC datacenter power design can improve data center energy efficiency by removing the need for an additional DC to AC inversion step.

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IBM System z

z10 EC Overview

- Machine Type
  - 2097
- 5 Models
  - E12, E26, E40, E56 and E64
- Processor Units (PUs)
  - 17 (17 and 20 for Model E64) PU cores per book
  - Up to 11 SAPs per system, standard
  - 2 spares designated per system
  - Dependant on the H/W model - up to 12, 26, 40, 56 or 64 PU cores available for characterization
    - Central Processors (CPs), Integrated Facility for Linux (IFLs), Internal Coupling Facility (ICFs), System z10 Application Assist Processors (zAAPs), System z10 Integrated Information Processor (zIIP), optional - additional System Assist Processors (SAPs)
- Memory
  - System Minimum of 16 GB
  - Up to 384 GB per book
  - Up to 1.5 TB for System and up to 1 TB per LPAR
    - Fixed HSA, standard
    - 16/32/48/64 GB increments
- I/O
  - Up to 48 I/O Interconnects per System @ 6 GBps each
  - Up to 4 Logical Channel Subsystems (LCSSs)
- ETR Feature, standard
Designed for improved server performance and scalability

- The z10 EC can deliver, on average, up to 50% more performance in an n-way configuration than an IBM System z9 Enterprise Class (z9 EC) n-way
  - The uniprocessor can deliver up to 62% more performance than z9 EC uniprocessor *
- The z10 EC 64-way can deliver up to 70% more server capacity than the largest z9 EC**
- Introducing HiperDispatch for improved synergy with z/OS® operating system to help deliver scalability and performance

* LSPR mixed workload average running z/OS 1.8 - z10 EC 701 versus z9 EC 701
** This is a comparison of the z10 EC 64-way and the z9 EC S54 and is based on LSPR mixed workload average running z/OS 1.8
* All performance information was determined in a controlled environment.
IBM System z: System Design Comparison

- **System I/O Bandwidth**
  - 288 GB/sec*
  - 172.8 GB/sec*
  - 96 GB/sec
  - 24 GB/sec
  - 16 GB/sec
  - 12 GB/sec
  - 8 GB/sec

- **Memory**
  - 1.5 TB**
  - 300 GB
  - 256 GB
  - 64 GB

- **ITR for 1-way**
  - 300
  - 250
  - 150

- **Balanced System CPU, nWay, Memory, I/O Bandwidth**
  - z10 EC
  - z9 EC
  - zSeries 990
  - zSeries 900

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*Servers exploit a subset of its designed I/O capability

** Up to 1 TB per LPAR
z10 BC Overview

- **Machine Type**
  - 2098

- **Single Model – E10**
  - Single frame, air cooled
  - Non-raised floor option available

- **Processor Units (PUs)**
  - 12 PU cores per System
  - 2 SAPs, standard
  - Zero spares when all PUs characterized
  - Up to 10 PUs available for characterization
    - Central Processors (CPs), Integrated Facility for Linux (IFLs), Internal Coupling Facility (ICFs), System z10 Application Assist Processors (zAAPs), System z10 Integrated Information Processor (zIIP), optional - additional System Assist Processors (SAPs)

- **Memory**
  - System Minimum of 4 GB
  - Up to 128 GB for System, including HSA (up to 256 GB, June 30, 2009)
    - 8 GB Fixed HSA, standard
    - Up to 120 GB for customer use (up to 248 GB, June 30, 2009)
    - 4, 8 and 32 GB increments (32 GB increment, June 30, 2009)

- **I/O**
  - Up to 12 I/O Interconnects per System @ 6 GBps each
  - 2 Logical Channel Subsystems (LCSSs)
  - Fiber Quick Connect for ESCON and FICON LX
  - New OSA-Express3 Features
  - ETR feature, standard
Designed with innovation for the modern enterprise

*Improved application performance and workload consolidation*

- The z10 BC can deliver up to 54% more performance for general purpose workloads than an IBM System z9 Business Class (z9® BC)*
- The uniprocessor can deliver up to 40% more performance than z9 BC uniprocessor **
- CPU intensive workloads get 2x performance improvements**
- Up to 10X improvement in decimal floating point instructions
- Up to 10 IFLs for large scale consolidation

All performance information was determined in a controlled environment.
* LSPR mixed workload average running z/OS® 1.9 - z10 BC z05 versus z9 BC z04  ** LSPR mixed workload average running z/OS 1.9 - z10 BC z01 versus z9 BC z01
z10 BC Configuration Comparisons

<table>
<thead>
<tr>
<th></th>
<th>z9 BC R07</th>
<th>z9 BC S07</th>
<th>z10 BC E10</th>
<th>z10 EC E12</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uniprocessor Performance</td>
<td>470 MIPS</td>
<td></td>
<td>673 MIPS</td>
<td>920 MIPS</td>
</tr>
<tr>
<td>System Capacity</td>
<td>26-172 MIPS</td>
<td>193-1748 MIPS</td>
<td>26-2760 MIPS</td>
<td>218-8225 MIPS</td>
</tr>
<tr>
<td>System Memory (with HSA)</td>
<td>Up to 64 GB</td>
<td>Up to 64 GB</td>
<td>Up to 256 GB (06/09)</td>
<td>Up to 384 GB</td>
</tr>
<tr>
<td>Configurable Engines</td>
<td>7</td>
<td>7</td>
<td>10</td>
<td>12</td>
</tr>
<tr>
<td>Configurable CPs</td>
<td>1-3</td>
<td>0-4</td>
<td>0-5</td>
<td>0-12</td>
</tr>
<tr>
<td>LPARS/LCSS</td>
<td>15/1</td>
<td>30/2</td>
<td>30/2</td>
<td>60/4</td>
</tr>
<tr>
<td>HiperSockets</td>
<td>16</td>
<td></td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>I/O Cages/Drawers</td>
<td>1</td>
<td>1</td>
<td>Up to 4</td>
<td>Up to 3</td>
</tr>
<tr>
<td>I/O slots per Cage/Drawers</td>
<td>16</td>
<td>28</td>
<td>8</td>
<td>28</td>
</tr>
<tr>
<td>FICON Channels</td>
<td>64</td>
<td>112</td>
<td>128</td>
<td>256</td>
</tr>
<tr>
<td>OSA Ports (10GbE/1GbE)</td>
<td>16/32</td>
<td>24/48</td>
<td>48/96</td>
<td>48/96</td>
</tr>
<tr>
<td>ESCON Channels</td>
<td>240</td>
<td>420</td>
<td>480</td>
<td>960</td>
</tr>
<tr>
<td>STI (z9), IFB (z10) Bandwidth</td>
<td>2.7 GB/sec</td>
<td></td>
<td>6.0 GB/sec</td>
<td>6.0 GB/sec</td>
</tr>
<tr>
<td>ICB-4/ISC-3/12x/1xPSIFB</td>
<td>16/48/12/12</td>
<td></td>
<td>12/48/12/12</td>
<td>16/48/16/16</td>
</tr>
<tr>
<td>zIIP/zAAP Maximum Qty</td>
<td>3</td>
<td>3</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>Capacity Settings</td>
<td>20</td>
<td>53</td>
<td>130</td>
<td>48</td>
</tr>
<tr>
<td>Upgradeable</td>
<td>Upgrade to z9 S07 and z10 BC</td>
<td>Upgrade to z9 EC &amp; z10 BC</td>
<td>Upgrade to z10 EC, Model E12</td>
<td>Upgrade to z10 EC E26, E40, E56 and E64</td>
</tr>
</tbody>
</table>
**z10 BC Sub-capacity Processor Granularity**

- The z10 BC has 26 CP capacity levels (26 x 5 = 130)
  - Up to 5 CPs at any capacity level
    - All CPs must be the same capacity level
- The one for one entitlement to purchase one zAAP and/or one zIIP for each CP purchased is the same for CPs of any speed.
  - All specialty engines run at full speed
  - Processor Unit Value for IFL = 120

### Table: Number of z10 BC CPs

<table>
<thead>
<tr>
<th>Number of CPs</th>
<th>Base Ratio</th>
<th>Ratio z9BC to z10BC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 CP</td>
<td>z9 BC Z01</td>
<td>1.40</td>
</tr>
<tr>
<td>2 CPs</td>
<td>z9 BC Z02</td>
<td>1.36</td>
</tr>
<tr>
<td>3 CPs</td>
<td>z9 BC Z03</td>
<td>1.30</td>
</tr>
<tr>
<td>4 CPs</td>
<td>z9 BC Z04</td>
<td>1.28</td>
</tr>
<tr>
<td>5 CPs</td>
<td>Z9 BC Z04</td>
<td>1.54</td>
</tr>
</tbody>
</table>
z10 EC Base and Sub-Capacity Offerings

- The z10 EC has 36 additional capacity settings at the low end.
- Available on ANY H/W Model for 1 to 12 CPs. Models with 13 CPs have to be full capacity.
- All CPs must be the same capacity within the z10 EC.
- All specialty engines run at full capacity. The one for one entitlement to purchase one zAAP or one zIIP for each CP purchased is the same for CPs of any capacity.
- Only 12 CPs can have granular capacity, other PU cores must be CBU or characterized as specialty engines.

CP Capacity
Relative to Full Speed
7xx = 100%
6xx ≈ 69%
5xx ≈ 51%
4xx ≈ 23%
xx = 01 Through 12
Mainframe Innovation: Specialty Engines

- Internal Coupling Facility (ICF) 1997
- Integrated Facility for Linux® (IFL) 2000
- System z Application Assist Processor (zAAP) 2004

Eligible for zAAP:
- Java execution environment
- z/OS XML System Services

Eligible for zIIP:
- DB2 remote access
- DB2 for BI/DW
- ISVs
- IPSec encryption
- z/OS XML System Services
- z/OS Global Mirror (XRC)
- HiperSockets for large messages
- IBM GBS Scalable Architecture for Financial Reporting
- z/OS CIM Server
- DB2 sort utility
- zAAP on zIIP

New! z/OS 1.11
IBM System z10 Upgrades
### z10 EC System Upgrades

- **z10 EC to higher hardware z10 EC model**
  - Upgrade of z10 EC Models E12, E26, E40 and E56 to E64 is disruptive
  - When upgrading to z10 EC E64, unlike the z9 EC, the first Book is retained
- **Any z9 EC to any z10 EC**
- **Any z990 to any z10 EC**
**z10 BC Upgrade Paths**

- Can enable dynamic and flexible capacity growth for mainframe servers
- Temporary capacity upgrade available through On/Off Capacity on Demand
- Temporary, nondisruptive addition of CP processors, IFLs, ICFs, zAAPs or zIIPs
- New options for reconfiguring specialty engines if the business demands it
- New options for changing On/Off CoD configurations
- Subcapacity CBU engines

- Full upgrades within the z10 BC
- Any to any upgrade from the z9 BC
- Any to any upgrade from z890
- No charge MES upgrades on IFLs, zAAPs and zIIPs
IBM System z10 Processor Structure
z10 EC Chip Relationship to POWER6™

- New Enterprise Quad Core z10 EC processor chip
- Siblings, not identical twins
- Share lots of DNA
  - IBM 65nm Silicon-On-Insulator (SOI) technology
  - Design building blocks:
    - Latches, SRAMs, regfiles, dataflow elements
  - Large portions of Fixed Point Unit (FXU), Binary Floating-point Unit (BFU), Hardware Decimal Floating-point Unit (HDFU), Memory Controller (MC), I/O Bus Controller (GX)
  - Core pipeline design style
    - High-frequency, low-latency, mostly-in-order
  - Many System z and System p® designers and engineers working together
- Different personalities
  - Very different Instruction Set Architectures (ISAs)
    - Very different cores
  - Cache hierarchy and coherency model
  - SMP topology and protocol
  - Chip organization
  - IBM z10 EC Chip optimized for Enterprise Data Serving Hub
z10 BC SCM and z10 EC MCM Comparison

z10 BC Single Chip Modules

- PU SCM
  - 50mm x 50mm in size – fully assembled
  - Quad core chip with 3 active cores
  - 4 PU SCMs per System with total of 12 cores
  - PU Chip size 21.97 mm x 21.17 mm

- SC SCM
  - 61mm x 61mm in size – fully assembled
  - 2 SC SCMs per System
  - 24 MB L2 cache per chip
  - SC Chip size 21.11 mm x 21.71 mm

z10 EC Multichip Module

- MCM
  - 96mm x 96mm in size
  - 5 PU chips per MCM
    - Quad core chips with 3 or 4 active cores
    - PU Chip size 21.97 mm x 21.17 mm
  - 2 SC chips per MCM
    - 24 MB L2 cache per chip
    - SC Chip size 21.11 mm x 21.71 mm
  - Up to 4 MCMs for System
Two new types of Single Chip Modules (SCMs)
- Processor – PU (4 SCM’s x 3 cores = 12 PU’s)
- System Controller – SC (2)

- 32x DIMM slots
- 2 Flexible Support Processor (FSP) card slots providing support for the Service Network subsystem (hot swappable)
- 6 fanout card slots providing support for the I/O subsystem and/or coupling
- 2 card slots for the oscillator/ETR function (standard) – dynamic switchover support

2 Air Moving Devices (not shown)
3 DCA’s
z10 BC – Under the covers Front View

- Power Supplies
- Internal Battery (optional)
- CPC (SCMs, Memory, MBA, HCA and FSP) Drawer
- 2 x Support Elements
- Fiber Quick Connect (FQC) Feature (optional – not shown)

I/O Drawer #1
I/O Drawer #2
I/O Drawer #3
I/O Drawer #4

4 x I/O Drawers
z10 EC Book Layout

Fanouts
- HCA2-O (InfiniBand)
- FSP cards
- HCA2-C (I/O cages)
- MBA (ICB-4)

Note: Chart shows an example of how and where different fanouts are installed. The quantities installed will depend on the actual I/O configuration.

HCA2-O LR fanout not shown
z10 EC – Under the covers (Model E56 or E64)

- Internal Batteries (optional)
- Power Supplies
- 2 x Support Elements
- 3x I/O cages
- Fiber Quick Connect (FQC) Feature (optional)
- Processor Books, Memory, MBA and HCA cards
- Ethernet cables for internal System LAN connecting Flexible Service Processor (FSP) cage controller cards
- InfiniBand I/O Interconnects
- 2 x Cooling Units
# z10 EC Orderable Processor Features and Memory

<table>
<thead>
<tr>
<th>Model</th>
<th>MCM size &amp; Qtys</th>
<th>PU cores</th>
<th>CPs</th>
<th>IFLs uIFLs</th>
<th>zAAPs</th>
<th>zIIPs</th>
<th>ICFs</th>
<th>Std SAPs</th>
<th>Std Spares</th>
<th>Standard Memory GB*</th>
<th>Flexible Memory GB</th>
</tr>
</thead>
<tbody>
<tr>
<td>E12</td>
<td>1 x 17</td>
<td>17</td>
<td>0 - 12</td>
<td>0 - 12 0 - 11</td>
<td>0 - 6</td>
<td>0 - 6</td>
<td>0 - 12</td>
<td>3</td>
<td>2</td>
<td>16 - 352</td>
<td>NA</td>
</tr>
<tr>
<td>E26</td>
<td>2 x 17</td>
<td>34</td>
<td>0 - 26</td>
<td>0 - 26 0 - 25</td>
<td>0 - 13</td>
<td>0 - 13</td>
<td>0 - 16</td>
<td>6</td>
<td>2</td>
<td>16 - 752</td>
<td>32 - 352</td>
</tr>
<tr>
<td>E40</td>
<td>3 x 17</td>
<td>51</td>
<td>0 - 40</td>
<td>0 - 40 0 - 39</td>
<td>0 - 20</td>
<td>0 - 20</td>
<td>0 - 16</td>
<td>9</td>
<td>2</td>
<td>16 - 1136</td>
<td>32 - 752</td>
</tr>
<tr>
<td>E56</td>
<td>4 x 17</td>
<td>68</td>
<td>0 - 56</td>
<td>0 - 56 0 - 55</td>
<td>0 - 28</td>
<td>0 - 28</td>
<td>0 - 16</td>
<td>10</td>
<td>2</td>
<td>16 - 1520</td>
<td>32 - 1136</td>
</tr>
<tr>
<td>E64</td>
<td>1 x 17 3 x 20</td>
<td>77</td>
<td>0 - 64</td>
<td>0 - 64 0 - 63</td>
<td>0 - 32</td>
<td>0 - 32</td>
<td>0 - 16</td>
<td>11</td>
<td>2</td>
<td>16 - 1520</td>
<td>32 - 1136</td>
</tr>
</tbody>
</table>

- A minimum of one CP, IFL, or ICF must be purchased on every model
- “uIFL” in the chart means Unassigned IFL, an IFL purchased but delivered as inactive
- One zAAP and one zIIP may be purchased for each CP purchased
- Optional SAP numbers not shown
- Memory Granularity for purchase increases with memory size: 16, 32, 48 or 64 GB
* Note: Fixed HSA is not included

* GB: Gigabyte
IBM System z10 Capacity and Performance
**z10 Capacity Planning in a nutshell**

Don’t use “one number” capacity comparisons!
Work with IBM technical support for capacity planning!
Customers can now use zPCR

The IBM Processor Capacity Reference (zPCR) is a free tool available for download that can be used to size your System z processors.

http://www-03.ibm.com/support/techdocs/atmastr.nsf/WeblIndex/PRS1381
z10 LSPR Measurements – New for October, 2008

Session 2115 – Brad Snyder, Wednesday 9:30 AM

LSPR update with z/OS 1.9

- **Multi-Image LSPR table**
  - z/OS-1.9 Multi-Image table is new (includes all System z families)
  - z/OS-1.8 Multi-Image table remains (does not include z10 BC)

- **Single-Image LSPR table**
  - All System z families are included
  - Capacity data for up to maximum of 64 CPs

Note: A new zPCR workload mix, **DI-Mix** (Data Intensive) has been added to complement the suggested workload mixes already carried in zPCR. This mix is intended to represent situations where the production workload qualifies for LoIO-Mix, but has data intensive characteristics resulting from significant exploitation of Data-in-Memory techniques.

- **Capacity planning tools affected**
  - zPCR
  - zCP3000
  - BWATOOL
  - zPSG
  - zTPM

- **z10 processor capacity for z/OS is represented with HiperDispatch turned on**
IBM System z10 HiperDispatch, Large Page Support, and LPAR Dynamic PU Reassignment
z10 HiperDispatch

Session 2248 – Bob Rogers, Tuesday 3:00 PM

- **HiperDispatch – System z10 unique function**
  - Dispatcher Affinity (DA) – New z/OS Dispatcher
  - Vertical CPU Management (VCM) – New PR/SM™ Support

- **Mitigate impact of scaling differences between processor and memory**
  - Access to memory and remote caches not scaling with processor speed
  - Increased performance sensitivity to cache misses in multi-processor system

- **Optimize performance by redispersing units of work to same processor group**
  - Keep processes running near their cached instructions and data
  - Minimize transfers of data ownership among processors / books

- **Tight collaboration across entire System z10 hardware/firmware/OS stack**
  - Concentrate logical processors around shared L2 caches
    - The z10 BC with its single drawer and L2 will get minimal benefit, if any, from HiperDispatch
  - Communicate effective cache topology for partition to OS
  - Dynamically optimize allocation of logical processors and units of work
z10 Large Page Support

Session 2248 – Bob Rogers, Tuesday 3:00 PM

- **Issue: Translation Lookaside Buffer (TLB) Coverage shrinking as % of memory size**
  - Over the past few years application memory sizes have dramatically increased due to support for 64-bit addressing in both physical and virtual memory
  - TLB sizes have remained relatively small due to low access time requirements and hardware space limitations
  - TLB coverage today represents a much smaller fraction of an application’s working set size leading to a larger number of TLB misses
  - Applications can suffer a significant performance penalty resulting from an increased number of TLB misses as well as the increased cost of each TLB miss

- **Solution: Increase TLB coverage without proportionally enlarging the TLB size by using large pages**
  - A Large Page requires no TLB entries for virtual address translation
  - Enhanced DAT on z10 translates the entire 1 MB page from its Segment-Table Entry

- **Benefit:**
  - Designed for better performance by decreasing the number of TLB misses that an application incurs
z10 EC LPAR Dynamic PU Reassignment

- PR/SM dynamic relocation of running processors to different processor cores
- Designed to optimize physical processor location for the current LPAR logical processor configuration
- Swap an active PU with a different active PU in a different book
  - Designed Benefit: Better L2 cache reuse
  - CP, zAAP, zIIP, IFL and ICF supported
  - Triggers: Partition activation/deactivation, machine upgrades/downgrades, logical processors on/off
- Designed to provide the most benefit for:
  - Multiple book machines
  - Dedicated partitions and wide partitions with HiperDispatch active
IBM System z10 Memory Structure
z10 EC Memory Offering and Assignment

- **Memory Granularity for ordering:**
  - 16 GB: Std - 16 to 256; Flex - 32 to 256
  - 32 GB: Std - 288 to 512; Flex - 288 to 512
  - 48 GB: Std - 560 to 944; Flex - 560 to 944
  - 64 GB: Std - 1008 to 1520; Flex - 1008 to 1136

- **16 GB separate fixed HSA standard**

- **Maximum Physical Memory:**
  - 384 GB per book, 1.5 TB per system
    - Up to 48 DIMMs per book
    - 64 GB minimum physical memory in each book

- **Physical Memory Increments:**
  - 32 GB – Eight 4GB DIMMs (FC #1604)
    Preferred if can fulfill purchase memory
  - 64 GB – Eight 8 GB DIMMs (FC #1608)
    Used where necessary

- **For Flexible Memory, if required, 16 GB “Pre-planned Memory” features (FC # 1996) are added to the configuration.**

<table>
<thead>
<tr>
<th>Model</th>
<th>Standard Memory GB</th>
<th>Flexible Memory GB</th>
</tr>
</thead>
<tbody>
<tr>
<td>E12</td>
<td>16 - 352</td>
<td>NA</td>
</tr>
<tr>
<td>E26</td>
<td>16 - 752</td>
<td>32 - 352</td>
</tr>
<tr>
<td>E40</td>
<td>16 - 1136</td>
<td>32 - 752</td>
</tr>
<tr>
<td>E56</td>
<td>16 - 1520</td>
<td>32 - 1136</td>
</tr>
<tr>
<td>E64</td>
<td>16 - 1520</td>
<td>32 - 1136</td>
</tr>
</tbody>
</table>
## z10 BC Memory Configuration, 4 - 120 GB

The table below shows the memory offering in GB, including memory with 8 GB HSA, physically plugged, and the number of cards plugged in 2 GB and 4 GB increments. Shaded memory sizes can be reached by concurrent LIC CC change from the next lower size.

<table>
<thead>
<tr>
<th>Memory Offering (GB)</th>
<th>Memory with 8 GB HSA</th>
<th>Physically Plugged</th>
<th># of cards plugged DIMM size</th>
</tr>
</thead>
<tbody>
<tr>
<td><em>Customer purchased memory</em></td>
<td>4 GB Purchase Increments</td>
<td>4 GB Purchase Increments</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>12</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>8</td>
<td>16</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>12</td>
<td>20</td>
<td>24</td>
<td>12</td>
</tr>
<tr>
<td>16</td>
<td>24</td>
<td>24</td>
<td>12</td>
</tr>
<tr>
<td>20</td>
<td>28</td>
<td>32</td>
<td>16</td>
</tr>
<tr>
<td>24</td>
<td>32</td>
<td>32</td>
<td>16</td>
</tr>
<tr>
<td>28</td>
<td>36</td>
<td>40</td>
<td>20</td>
</tr>
<tr>
<td>32</td>
<td>40</td>
<td>40</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>8 GB Purchase Increments</td>
</tr>
<tr>
<td>40</td>
<td>48</td>
<td>48</td>
<td>24</td>
</tr>
<tr>
<td>48</td>
<td>56</td>
<td>56</td>
<td>28</td>
</tr>
<tr>
<td>56</td>
<td>64</td>
<td>64</td>
<td>32</td>
</tr>
<tr>
<td>64</td>
<td>72</td>
<td>80</td>
<td>0</td>
</tr>
<tr>
<td>72</td>
<td>80</td>
<td>80</td>
<td>0</td>
</tr>
<tr>
<td>80</td>
<td>88</td>
<td>96</td>
<td>0</td>
</tr>
<tr>
<td>88</td>
<td>96</td>
<td>96</td>
<td>0</td>
</tr>
<tr>
<td>96</td>
<td>104</td>
<td>112</td>
<td>0</td>
</tr>
<tr>
<td>104</td>
<td>112</td>
<td>112</td>
<td>0</td>
</tr>
<tr>
<td>112</td>
<td>120</td>
<td>128</td>
<td>0</td>
</tr>
<tr>
<td>120</td>
<td>128</td>
<td>128</td>
<td>0</td>
</tr>
</tbody>
</table>

Sizes shaded in green can be reached by concurrent LIC CC change from the next lower size.
### z10 BC Memory Configuration, 152 - 248 GB

<table>
<thead>
<tr>
<th>Memory Offering (GB) <em>Customer purchased memory</em></th>
<th>Memory with 8 GB HSA</th>
<th># of cards plugged DIMM size (GB) 8 GB</th>
<th>Physically Plugged</th>
</tr>
</thead>
<tbody>
<tr>
<td>152</td>
<td>160</td>
<td>20</td>
<td>160</td>
</tr>
<tr>
<td>184</td>
<td>192</td>
<td>24</td>
<td>192</td>
</tr>
<tr>
<td>216</td>
<td>224</td>
<td>28</td>
<td>224</td>
</tr>
<tr>
<td>248</td>
<td>256</td>
<td>32</td>
<td>256</td>
</tr>
</tbody>
</table>

**Note:** The above memory options became available in May, 2009
z10 Concurrent Memory Upgrades

**System z10 EC and BC**
- MES Change to LIC CC to enable additional memory to the physical limit of the installed cards and memory configuration
  - Designed to possible if **Plan Ahead Memory** has been ordered
  - May be possible and concurrent in some other configurations

**System z10 Enterprise Class**
- Add a book with additional memory
  - Designed to be possible except for Models E56 and E64

- Multiple book machines can exploit **Enhanced Book Availability** to change memory card configuration in existing books
  - Exploits the capability to remove, upgrade and return a book concurrently
  - Designed to be possible without disruption if **Flexible Memory** and some unassigned PUs are available in the configuration
  - May be possible without disruption with standard memory and/or limited unassigned PUs depending on LPAR configuration and workload
  - Customer pre-planning required may require acquisition of additional hardware resources
  - **Not possible on Model E12**

**Note:** Concurrent memory upgrades above are designed not to require CEC activation (POR). z/OS or z/VM with “reserved memory” configured in the LPAR profile can add memory to a running partition. Otherwise adding memory to a partition requires deactivation, profile change and activation of the partition. This is designed not to be disruptive to other partitions.
z10 BC and EC Plan Ahead Memory

- **Provides the ability to plan for non-disruptive memory upgrades**
  - Memory cards are pre-installed based on planned target capacity
- **Pre-installed memory is activated by installing a new LICCC**
  - Orderable via Resource Link by the customer (CIU upgrade)
  - Orderable as an ordinary MES by IBM
  - Memory upgrade orders use the pre-installed memory first
- **Pre-planned memory feature**
  - Charged when physical memory is installed and used to track the quantity of physical increments of plan ahead memory capacity
    - Cost part pre-paid
  - Increment size of based on minimum memory purchase increment
- **Pre-planned memory activation feature**
  - Charged when Plan Ahead Memory is enabled based on the amount of Plan Ahead memory that is being activated
    - Remaining cost paid at time of activation
  - Subsequent memory upgrade orders will use up the Plan Ahead memory first
- **Plan Ahead Memory is NOT temporary CoD or CBU memory**
  (Removing memory is disruptive)
IBM System z10 Capacity on Demand (CoD)
z10 – Basics of CoD

Capacity on Demand

Permanent Upgrade

Temporary Upgrade

Replacement Capacity

Billable Capacity (On/Off CoD)

Pre-paid

Post-paid

Using pre-paid unassigned capacity up to the HWM limit
No expiration
Capacity
- MSU %
- # Engines

On/Off CoD with tokens
No expiration
Capacity
- MSU %
- # Engines
Tokens
- MSU days
- Engine days

On/Off CoD with tokens
180 days expiration
Capacity
- MSU %
- # Engines
Tokens
- MSU days
- Engine days

Permanent Upgrade

Temporary Upgrade

Replacing Capacity

Billable Capacity

Pre-paid

Post-paid
## Capacity on Demand Comparisons – z9 vs z10

<table>
<thead>
<tr>
<th></th>
<th>System z9</th>
<th>System z10</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Resources</strong></td>
<td>CP, zIIP, zAAP, IFL, ICF</td>
<td>CP, zIIP, zAAP, IFL, ICF, SAP</td>
</tr>
<tr>
<td><strong>Offerings</strong></td>
<td>Requires access to IBM/RETAIN® to activate</td>
<td>No password or access to IBM/RETAIN required to activate</td>
</tr>
<tr>
<td></td>
<td>CBU, On/Off CoD</td>
<td>CBU, On/Off CoD, CPE</td>
</tr>
<tr>
<td></td>
<td>One offering at a time</td>
<td>Multiple offerings active</td>
</tr>
<tr>
<td><strong>Permanent upgrades</strong></td>
<td>Requires de-provisioning of temporary capacity first</td>
<td>Concurrent with temporary offerings</td>
</tr>
<tr>
<td><strong>Replenishment</strong></td>
<td>No</td>
<td>Yes with CBU &amp; On/Off CoD</td>
</tr>
<tr>
<td><strong>CBU Tests</strong></td>
<td>5 tests per record</td>
<td>1 per contract year (default) but can add more (15 max per record)</td>
</tr>
<tr>
<td><strong>CBU expiration</strong></td>
<td>Contract expiration, no record expiration</td>
<td>Contract and record expiration with term length up to 5 years</td>
</tr>
<tr>
<td><strong>Capacity Provisioning Manager support</strong></td>
<td>No</td>
<td>Yes (On/Off CoD)</td>
</tr>
</tbody>
</table>
IBM System z10 Cryptography
z10 CP Assist for Cryptographic Functions (CPACF)

Integrated Cryptographic Service Facility (ICSF)

Crypto Express2 CP Assist for Cryptographic Function

High performance clear key symmetric encryption/decryption
IBM System z10 BC Availability
z10 EC Enhancements designed to avoid Outages

- Continued Focus on Firmware Quality
- Reduced Chip Count on MCM
- Memory Subsystem Improvements

- DIMM FRU indicators
- Single Processor Core Checkstop
- Single Processor Core Sparing
- Point-to-Point SMP Fabric (not a ring)
- Rebalance PSIFB and I/O Fanouts
- Redundant 100Mb Ethernet service network w/ VLAN

NEW for z10 EC
- Plan ahead memory
- Serviceability enhancements of SAN for both FICON and FCP

- Reduce Pre-planning to Avoid POR
  - “Fixed” HSA amount
  - Dynamic I/O Enabled by Default
  - Add Logical Channel Subsystem (LCSS)
  - Change LCSS Subchannel Sets
  - Add/Delete Logical Partitions

- Reduce Pre-Planning to Avoid LPAR Deactivate
  - Change Partition Logical Processor Config
  - Change Partition Crypto Coprocessor Config

- CoD – Flexible Activation/Deactivation
  - Elimination of unnecessary CBU passwords

- Enhanced Driver Maintenance (EDM) Upgrades
  - Multiple “from” sync point support
  - Improved control of channel LIC levels
IBM System z10 BC I/O Connectivity
FICON, OSA, ESCON and Coupling Links

z10 I/O Connectivity:
Session 2214 – Lou Ricci, Tuesday 1:30 PM
Session 3166 – Newsom/Nusbaum/Seitz, Thursday 4:30 PM

Parallel Sysplex:
Session 2207 – Mark Brooks, Thursday 11:00 AM
and others
z10 Channel Type and Crypto Overview - July, 2009

- **FICON/FCP**
  - *FICON Express* \( \text{\textcolor{red}{new!}} \)
    - FICON Express4 2C (2-port – z10 BC only)
    - FICON Express4 (4-port features – CF on upgrade after withdrawal from marketing on 10/27/2009)
    - FICON Express2 (CF on upgrade)
    - FICON Express (CF on upgrade, LX for FCV)
- **Networking**
  - OSA-Express3
    - 10 Gigabit Ethernet LR and SR
    - Gigabit Ethernet LX and SX
    - 1000BASE-T Ethernet
  - OSA-Express2
    - 1000BASE-T Ethernet (For a limited time)
    - Gigabit Ethernet LX and SX (CF on upgrade)
    - 10 Gigabit Ethernet LR (CF on upgrade)
  - HiperSockets (Define only)
- **ESCON** – (no change)
- **Coupling Links**
  - InfiniBand Coupling Links
    - 12x IB DDR
    - 1x IB DDR
  - ISC-3 (Peer mode only)
  - ICB-4 (Not available on Model E64)
  - IC (Define only)
- **Crypto**
  - Crypto Express2
    - Configurable Coprocessor or Accelerator
- **Channel types not supported:**
  - FICON (pre FICON Express)
  - OSA-Express (pre OSA-Express2)
  - ICB-3

Note: ICB-4 cables are available as features. All other cables are sourced separately.
Improvements with System z10 and FICON Express8

- **z10 High Performance FICON for System z (zHPF)**
  - Simplification of storage area network (SAN) traffic with can improve performance
  - For small data transfers of OLTP and other workloads that exploit the zHPF protocol, the maximum number of I/Os per second is increased by up to 100%*
  - zHPF only available on System z10
    - Supported on FICON Express8, FICON Express4 and FICON Express2
    - z/OS V1.7 with the IBM Lifecycle Extension for z/OS V1.7 (5637-A01), V1.8, V1.9, or V1.10 with PTFs
    - Control unit exploitation - IBM System Storage DS8000 Release 4.1

- **FICON Express8**
  - Another System z10 exclusive
  - Supports an 8 Gbps link data rate with autonegotiation to 2 or 4 Gbps

**FICON performance on System z – MBps throughput**
- **zHPF – 40% increase FICON Express8 vs. FICON Express4**
- **FICON – 45% increase FICON Express8 vs. FICON Express4**

**FICON performance on System z – start I/Os**
- **zHPF – 70% increase FICON Express8 vs. FICON Express4**
- **FICON – 40% increase FICON Express8 vs. FICON Express4**

*This performance data was measured in a controlled environment running an I/O driver program under z/OS. The actual throughput or performance that any user will experience will vary depending upon considerations such as the amount of multiprogramming in the user's job stream, the I/O configuration, the storage configuration, and the workload processed.