

Product Quality Addendum [PQA] for Purchased Electronic Components

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1. Scope:

This specification defines IBM's commodity specific requirements for purchased electronic components, by IBM or IBM authorized sub-contractors. This document is to be used in conjunction with IBM specification 03N6596, "IBM Supplier Quality Requirements Document (SQRD)". This specification defines additional commodity specific requirements as an addendum to the SQRD. The major section numbers, from section 3 onward, of this document correspond to the major sections of the SQRD.

1.2 Applicability:

To be applicable, this specification shall be referenced by an IBM Part Number, or applicable procurement document and shall apply to all purchases made under that Part Number by IBM, IBM's Affiliates, or any third parties purchasing the product to IBM's part number.

2. General:

2.1 Definitions:

Assembly	A part consisting of one or more components and or modules.
AVL	"Approved Vendor List" is a list of authorized/qualified Suppliers.
BGA	"Ball Grid Array".
BTR	"Business/Technical Review"
CGA	"Column Grid Array"
CoO	"Country of Origin".
Component	A part which is not considered an assembly.
CVS	"Cyclic Voltammetry Stripping"
DIMM	"Dual Inline Memory Module"
DRAM	"Dynamic Random Access Memory"
EOL	"End Of Life", also know as Component Discontinuance
ESI	"Electronic Supplier Interchange".
FAI	"First Article Inspection"
IBM	"International Business Machines".
IVH	"Inter Via Hole"

ESD	“Electro Static Discharge”.
HIC	“Humidity Indicator Card” used to monitor moisture absorption for moisture sensitive components (see J-STD-033).
Module	A part which is constructed of multiple components on a substrate (also see “Subassembly”).
MRB	“Material Review Board”
N/A	“Not Applicable”, used to indicate that the item does not apply and also was not an accidental omission.
NSMD	“Non-Solder Mask Defined”
Package	“ The materials and construction that make up a component”
PCD	“Product Content Declaration”
PCN	“Process Change Notice”.
PGA	“Pin Grid Array”
PQA	The “Product Quality Addendum” is an optional document, provided by the Buyer to the Supplier, that sets forth specific quality requirements for a Product including technical, and or quality goals for the Product and any exceptions to the SQRD document.
PTH	“Pin Through Hole”
PWB/PCB	“Printed Wiring Board/Printed Circuit Board” is the substrate material to which other component are attached in an assembly, also know by the term “raw card”.
QFP	“Quad Flat Pack”
RoHS	“Reporting of Hazardous Substances”. See IBM specification 46G3772 for further definition.
SAC	Tin-Silver-Copper Alloys, derived from the from the first element abbreviation letters (SnAgCu).
SMD	“Solder Mask Defined”
SMT	“Surface Mount Technology”
SPEX	The “Supplier Part Number Exchange” system provides information on IBM part numbers to Suppliers.
SPC	“Statistical Process Control”
SQD	The “Supplier Quality Document” is an optional document, provided by the Supplier to the Buyer, that documents any or all of the following, as applicable: <ul style="list-style-type: none"> • Supplier’s commitments and methods to meet all quality requirements of the SQRD documents and the PQA. • Buyer Approved Waivers / Specification exceptions. • Supplier’s Quality and Reliability commitments.
SPQL	“Shipped Product Quality Level” is the quality level as seen at the next level of manufacturing or assembly.

- SQR “Supplier Quality Review”.
- SQRD The “Supplier Quality Requirements Document” (03N6596). outlines the minimum Supplier quality and process requirements for supplying Products to IBM or Authorized Third Parties.
- SRR “Supplier Readiness Review” is a business/technical review between IBM and a Supplier to review the Suppliers ability to support IBM program(s).
- Subassembly (see “Module”).

2.2 Precedence:

In case of conflict between IBM requirements, the order of precedence provisions set forth in the Applicable agreement shall apply. In the event of an inconsistency in the technical requirements, the following order of precedence shall apply:

- IBM Written Waivers (mutually agreed in writing)
- IBM Part Number Drawing (or equivalent component description documentation)
- IBM SQD
- This Specification
- IBM SQRD
- Other IBM Specifications
- Referenced Industry Standards
- Supplier Technical Specifications - (including such items as: electrical performance specs, quality and reliability commitments etc.)

2.3 Referenced Documents:

IBM Specification 03N6596 “SQRD” shall apply to any component referencing this specification. IBM specifications 77P0594 and or 26P0381 shall apply when referenced by the IBM [part number](#) drawing or equivalent IBM component description documentation, including [IBM’s SPEX system](#).

The following documents in their current revision or successor shall form a part of this specification to the extent specified in the body of the document. In case of conflict see Section 2.2 “Precedence”.

IBM Document Number	IBM Document Title
03N6596	IBM Supplier Quality Requirements Document (SQRD)
26P0381	IBM Environmental Lead(Pb)-Free Requirements for Purchased Electronic Components. (including Restriction on Hazardous Substances RoHS)
46C3484	Product Content Declaration for IBM Suppliers
46G3772	Baseline Environmental Requirements for Materials, Parts and Products for IBM Logo Hardware Products
53P4082	Generic Quality, Reliability and Performance Specification for IBM Systems Group Rigid Printed Circuit Boards
61X5956	Printed Circuit Tab Requirements for Wiping Contacts (applicable only to modules with edge connectors)
77P3021	Additions, Exceptions and Limitations to Industry Standards for IBM Memory DIMMs
77P0594	IBM Server and Storage System’s Environmental Requirements for Purchased Electronic Components Used in a Leaded(Pb) Solder System . (including Restriction on Hazardous Substances RoHS)

92F6933	Packaging Requirements for Dangerous Goods
C-S 1-1121-003	Information Plates and Labels (IBM)
C-S 3-0501-070	Product Safety, IBM Requirements: Electrical, Mechanical, Flammability

Industry Document Number	Industry Document Name
EIA 186-6	Mechanical Robustness of Terminals
EIA 186-13	Insulation Resistance Test
EIA-296	Lead Taping of Components in Axial Lead Configuration for Automatic Handling
EIA-468	Lead Taping of Components in Radial Configuration for Automated Assembly
EIA-481	8 mm through 200 mm Embossed Carrier Taping and 8 mm & 12 mm Punched Carrier Taping of Surface Mount Components For Automatic Handling
EIA 476	Date Code Marking
EIA-541	Packaging Material Standards for ESD Sensitive Items
EIA 599	National Electronic Process Certification Standard (NECQ)
EIA-763	Bare Die and Chip Scale Packages Taped in 8 mm and 12 mm Carrier Tape for Automatic Handling
IEC-60068-2-6	Environmental testing - Part 2-6: Tests - Test Fc: Vibration (sinusoidal)
IPC-A-600	Acceptability of Printed Boards
IPC-A-610	Acceptability of Electronic Assemblies
IPC-7711	Rework of Electronic Assemblies
IPC-9502	PWB Assembly Soldering Process Guideline for Electronic Components
IPC 9503	Moisture Sensitivity Classification for Non-IC Components
IPC-9504	Assembly Process Simulation for Evaluation of Non-IC Components
ISO 2859	Sampling Procedures for Inspection by Attributes
ISO 3951	Sampling Procedures for Inspection by Variables
ISO 9001	Quality Management Systems - Requirements
J-STD-001	Requirements for Soldered Electrical And Electronic Assemblies
J-STD-002	Solderability Requirements for Electronic Components
J-STD-004	Requirements for Soldering Fluxes
J-STD-005	Requirements for Soldering Pastes
J-STD-020	Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
J-STD-033	Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices
J-STD-075	Classification of Non-IC Electronic Components for Assembly Processes
JESD22-A104	Temperature Cycling
JESD22-A109	Hermeticity
JESD22-A113	Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
JESD22-A114	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
JESD22-B101	External Visual
JESD22-B103	Vibration, Variable Frequency
JESD22-B104	Mechanical Shock
JESD22-B105	Lead Integrity
JESD22-B106	Resistance to Soldering Temperature for Through Hole Mount Devices
JESD22-B107	Marking Permanency
JESD22-B114	Mark Legibility

JESD22-B115	Solder Ball Pull
JESD22-B117	BGA Ball Shear
JESD22-C101	Field Induced Charged Device Model ESD Testing
JESD 38	Standard for Failure Analysis Report Format
JESD 46	Customer Notification of Product/Process Changes by Semiconductor Suppliers
JESD 48	Product Discontinuance
JESD 50	Special Requirements for Maverick Product Elimination and Outlier Management
JESD 69	Information Requirements for the Qualification of Silicon Devices
JEP 95	JEDEC Registered and Standard Outlines for Solid State and Related Products
JESD 625	Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
JESD 659	Failure-Mechanism-Driven Reliability Monitoring
JESD 671	Component Quality Problem Analysis and Corrective Action Requirements
JIS-C-5101-1	Fixed capacitors for use in electronic equipment. Part 1: Generic specification
JIS-C-5201-1	Fixed resistors for use in electronic equipment -- Part 1: Generic specification
MIL-STD 202	Test Methods for Electronic and Electrical Component Parts
MIL-STD 883	Test Methods and Procedures for Microelectronics
UL94	Tests for Flammability of Plastic Materials for Parts in Devices and Appliances
UL1694	Tests for Flammability of Small Polymeric Component Materials

Copyrighted standards referenced above are available through many sources, including the following:

Agency (Abbreviation) Name	INTERNET Address
Electronic Industries Alliance (EIA)	http://www.eia.org
International Electrotechnical Commission (IEC)	http://www.iec.ch
IPC	http://www.ipc.org
International Organization for Standardization (ISO)	http://www.iso.org
Joint Electron Device Engineering Council (JEDEC)	http://www.jedec.org
Japanese Standards Association (JIS)	http://www.jsa.or.jp/default_english.asp
Underwriters Laboratories (UL)	http://www.ul.com

2.4 Exceptions:

Any exception to the requirements of this specification shall constitute a change that must be approved in writing by IBM and documented in an [SQD](#).

2.5 IBM Part Number Alterations and Additions:

The Supplier Quality Document is maintained and controlled by IBM Procurement Engineering. Any change requests must be submitted in writing to the IBM Procurement Engineer. Alterations must be mutually agreed upon by the Supplier and IBM.

IBM and Supplier agree that the definition of IBM [Corporate approved and managed](#) part numbers will be communicated via e-mail using a process called SPEX. Under SPEX, IBM [delivers](#) two (2) part number drawing files per week by e-mail. These part number drawing files describe all pre-existing IBM part numbers as well as any new part number adds/changes that occurred over the last seven days. [This process does not apply to IBM Divisionally managed/locally released part numbers.](#) For each part number, this file will include, but not be limited to, the following information about the part number:

FILE COLUMNS	EXPLANATION
IBM Part Number	IBM Part Number
Supplier Part Number	Supplier part number published in supplier catalog
Product Rev Level	Applies to the following Logic components: ALDC, ATM, Controllers, Bus/Driver/Interface, Serial Port, Core Logic, Crypto Chips, Custom Processors, Digital Signal Processors, Ethernet, FDDI, Graphics/Video, Hub/Bridge Chips, MPEG, Microassemblies, Microcontrollers, Modem Modules, Other Microprocessors, Other Network Products, Other Peripherals, Power PC Microprocessors, Super IO, X86 Microprocessors
Commodity	Generic description/categorization of part
Additional IBM Requirements	Deltas to published Supplier part number specifications and/or additional IBM test requirements. This may include burn-in conditions, tighter electrical specs or other special reqs.
Applicable IBM Specifications	Generic IBM Specs (873444, 03N6596 , others if needed)
Applicable RoHS Specifications	IBM ROHS /Lead(Pb)-free spec that the part number must comply with (26P0381, 77P0594, other if needed)
Responsible IBM Engineer	Procurement engineer's name
Create Date	Date when the record was first entered into IBM's database
Add / Change Date	Date that the record first appeared in this file or the date when the record was last changed, which ever date is more recent.
Supplier Name	Name of the supplier

Supplier shall have seven (7) calendar days to reject any additions or changes. [Supplier rejections must be in writing](#). If Supplier fails to reject such changes within the seven (7) day period, such changes or additions shall be deemed to have been accepted. [Once each year, IBM shall request the Supplier review](#) and sign off on the most recent IBM Part Numbers Drawing file that is in effect. [The most current part number information shall supersede all previous IBM SPEX part number information](#).

3. Introduction:

There are no additional commodity specific requirements in addition to those stated in the [Introduction section of the SQRD \(03N6596\)](#).

4. Manufacturing Qualification and Process Control:

4.1 Process / Product Monitoring:

Suppliers shall analyze part failures returned by IBM, Third Parties purchasing the IBM part number or those [failures](#) detected by the Supplier or Supplier's sub contractor. This information will be fed back into their Product processes with the goal of defect elimination on each and every manufacturing line. If elimination of the Supplier's defect cannot be immediately achieved, the Supplier's execution of an IBM approved containment plan shall be an interim goal. This analysis information includes determination of failure mechanism, defect point of origin (process step), magnitude of each mechanism's contribution to overall Quality or Reliability, and prioritization of improvement efforts based on magnitude of contribution and impact on customer. Techniques for generation of information may include, but are not limited to, the following:

- Periodic construction analysis
- Ongoing Reliability Monitor program (per JESD 659)
- Failure analysis of :
 - Customer returns
 - Reliability monitor failures (on actual product)
 - Burn-in and/or voltage-screen failures
 - Statistically low or high yielding lots (failing **components** and or wafers, see ISO 2859)
 - Normal-yielding lots (failing **components** and or wafers)
 - In-line test or in-line monitor failures (see ISO 3951)
 - Wafer-level- and assembly-level-reliability test structure failures
 - In-line inspection defects
 - Raw Materials
 - Nonconforming materials

Each Supplier will be required to generate a Quality Pareto diagram in addition to the Reliability Pareto of failure mechanisms required by JESD 659 and describe an appropriate improvement plan for the top items for each Pareto. This plan shall include implementation schedules for corrective actions. The measurement plan must demonstrate with high confidence that the expected improvement is being achieved. The measurements should be installed at the process point at which a meaningful indicator of improvement can be achieved. This information shall be reviewed upon request.

4.2. Maverick Product Elimination (MPE) Program:

Component quality and reliability performance currently being achieved by the electronic component industry is such that product anomalies become major impacts to the end user. These situations are called "Maverick Product". These anomalies can occur in any commodity and can significantly impact the expected performance of the commodity. The causes of the "Maverick Product" can vary across the entire spectrum of processes including, but not limited to, fabrication, assembly, test, **packing**, and handling operations.

The primary consideration is to protect the customer from the potential impact of processing variation anomalies. Problem prevention is accomplished by eliminating atypical product, and by using failure mechanism based product monitors, process controls and user data. Suppliers shall review their MPE plans with IBM during the Supplier Quality Review (SQR) or upon request. IBM recommends that the "best practice" industry standard "EIA JESD 50" be used.

The Supplier's MPE program shall include:

A) Identification of Abnormal Events: A methodology shall be in place which uses valid and effective statistical methods to identify abnormal events at all stages of the manufacturing process which affect product quality and reliability, including:

- Incoming materials, materials storage, and materials distribution
- In-line fabrication processes
- Parametric test (a.k.a. acceptance test, kerf test, electrical test)
- Sort test (a.k.a. functional test, final test)

B) Identification of Suspect Material: A methodology must be in place which ensures that for every abnormal event identified in A), above, all production material which could be affected by that abnormal event is identified. This material is to be considered suspect material until it receives adequate technical evaluation per C), below.

C) Evaluation of suspect material: A methodology must be in place which ensures all suspect material identified in B), above, is given adequate technical evaluation to determine if the material is expected to have the same quality and reliability characteristics as normal production material.

Adequate technical evaluation must be done:

- Only by personnel who have documented organizational authority to make such evaluations.
- Only by personnel who are recognized by the organization as subject-matter experts in quality and reliability.
- With clear and explicit documentation, including:
 - The outcome of the evaluation, e.g., the material is (or is not) expected to have the same quality and reliability characteristics as normal production material
 - Who made the evaluation: employee name(s) and organizational title(s)
 - Date of the evaluation
 - Data that were used to make the evaluation (e.g., test data, inspection data, other measurement data)

Suspect material which has received adequate technical evaluation, and which is expected to have the same quality and reliability characteristics as normal production material, may only be shipped to IBM with IBM written approval..

Suspect material for which adequate technical evaluation does not result in confidence that the material is expected to have the same quality and reliability characteristics as normal production material is to be considered maverick material, and must not be shipped to IBM without prior written approval from IBM.

See section 6.14.4.5 for additional requirements for IBM Custom DIMMs.

4.2.1 Allowable Rework:

4.2.1.1 Component Package Rework:

No component package rework is allowed, except for the following:

1. Second pass solder plate to ensure thickness
2. Lead straightening (both "combing" and "reforming"), as long as the lead finish is not damaged.
3. Remark (Ink only) prior to ink cure.
4. Solder ball attach (ceramic BGA only).
5. Solder ball attach prior to reflow (Plastic BGA)

If a supplier requests rework to perform 2nd reflow to attach a few missing BGA balls, the supplier must then precondition (JESD22-A113) their product with a fourth SMT reflow passes prior to their reliability qualification testing.

All other rework operations are not allowed without written IBM approval. (IBM approval will require a documented rework flow and qualification results).

4.2.1.2 Silicon Fabrication Rework:

No rework is allowed, except for the following:

1. Removal and re-application of photoresist, as part of a standard documented procedure for photo rework.

All such rework must be documented by the same means, and with the same level of detail, as all other normal fab processing operations. There must be a documented limit on the number of times a lithographic operation may be reworked before the entire affected wafer lot is put on hold for root-cause analysis and engineering disposition.

2. Additional ion implantation, in cases where ion implantation was interrupted and reliable dose-counter measurements are available to set the required additional dose.

All such rework must be documented by the same means, and with the same level of detail, as all other normal fab processing operations.

All other rework operations are not allowed without written IBM approval. IBM approval will require a documented rework flow and qualification results.

4.2.1.3 Passive and Other Component Rework:

No additional rework is allowed.

All other rework operations are not allowed without written IBM approval. IBM approval will require a documented rework flow and qualification results.

4.2.1.4 Module Assembly Rework:

This applies to Memory DIMM's, fiber optic transceivers, magnetic filters and other assemblies.

No rework is allowed, except for the following:

1. Rework of any single DRAMs is limited to one time only.
2. A maximum of 3 different component site reworks are permitted per DIMM. Reworked components must be marked for traceability.
3. A Surface Mount component site may be reworked/touched-up no more than 2 times using methods stated in IPC-7711 or an IBM approved alternative method. The reworked site must pass the visual inspection requirements as stated in this specification.

Printed Wiring Board (PWB) rework, including gold plate rework, is not permitted unless specifically approved by IBM.

For Surface Insulation Resistance testing, simulate rework by: applying primary paste and rework flux; reflow; and cleaning process (where used).

4.3 Product Traceability:

Component carrier/module marking must be maintained by the Supplier for all product to enable identification of the product back to all plants of manufacture (fab, assembly, and test locations), manufacturing process within a plant, as well as fabrication, assembly and test lots (eg. Date Code). For electronic components with serial numbers, traceability to the serial numbers is preferred.

The Supplier must document their marking scheme format, per package/pin count and submit this information to the IBM purchasing organization for reference.

Parts must be marked in accordance with the applicable IBM specifications. In addition, the Supplier must be able to trace volumes, manufacturing lot numbers and quantities shipped to any IBM or IBM authorized subcontractor location (forward traceability), and from the marking on a defective component (on its packing for very small parts like SMT Passive) back to the manufacturing lot (backward traceability).

Where IBM part number(s) is being purchased by third parties, the product traceability requirements shall apply to all purchasers of the IBM part number and traceability data for such third party's purchases shall be made available to IBM. See section 6.14.4.2 for additional requirements for IBM custom DIMMs.

4.4 First Piece Build and Inspection Requirements:

Per the SQRD (IBM specification 03N6596) section 4.5, the data shall be available upon IBM request.

5. Process / Product / Engineering Change Controls:

There are two types of Process Change Notices (PCNs) sent to IBM. "Execute PCNs" are PCNs where all the required information, data and Product samples (outlined in section 5.1) are currently available from the Supplier.

Qualification data shall include an analysis of the reliability data including the methodology used in the reliability calculations, a comparative electrical characteristic analysis and manufacturing line equivalency analysis for product line additions or moves. "Advance Notice PCNs" are PCN's where one or more of the required information, data or Product samples are not available, but the Supplier wishes to give IBM advance visibility to a Supplier's potential process change. Suppliers shall notify IBM of any reportable material changes (see IBM specification 46G3772), in addition to the listed set of changes outlined in section 5.3 of the SQRD.

Suppliers shall also meet the requirements in JESD 46 with the following exceptions:

1. Notification is required on all IBM part numbers regardless of the purchase activity level, and only applies to components for which the Supplier had not already discontinued the component per section 5.3.
2. Suppliers shall provide IBM annually the definition of the "major" vs. "minor" process changes per JESD 46.

For any Ball Grid Array (BGA) metallurgy changes from leaded(Pb) balls to lead(Pb)-free balls, the Supplier shall submit an End of Life (EOL) notice instead of a PCN.

5.1 Execute PCNs:

Per section 5.3 of the SQRD, PCNs require written notification to [or submission through IBM's Electronic Supplier Interchange (ESI) system] an IBM representative at least three months (90 days) in advance of any such changes. The following non proprietary information data shall be included for Execute PCNs:

- Supplier PCN Number
- Supplier Contact Information (e.g. Contact name, phone, fax and e-mail)
- Type of PCN as one of the following general categories:
 - Pb-Free Assembly/Material/Package change
 - Fab Site Change - Previously qualified by IBM
 - Assembly Site Change - Previously qualified by IBM
 - Fab Site Change - Not previously qualified by IBM
 - Assembly Site Change - Not previously qualified by IBM
 - Burn-in Change
 - Assembly/Material/Package change (May require a new materials declaration submission)
 - Mask/Design change or shrink
 - Change to Fab Process
 - Test Program Change
 - 1st level container change (Tray/T&R/Tube/etc.)
 - Packing/label/component marking change
 - Package Process Change
 - Dimensional change to package
 - Circuit or Specification Change
 - Other. Describe in Comment Section
 - Test/Burn-in Site Change

Additional for Logic Commodity Only general categories:

- Data sheet/Errata change
- Stepping Change

Additional for Memory Commodity Only general categories:

- PCB layout change (SIMM / DIMM)
- PCB supplier change (SIMM / DIMM)
- Change to buffers on SIMM/DIMM
- Change to EEPROM on SIMM / DIMM
- Miscellaneous SIMM / DIMM change
- Data sheet/Errata change

- Commodity
- Date when IBM response is requested
- Supplier Name
- Is there a specification change? (Y/N)
- Original Supplier part numbers
- New Supplier part numbers (if applicable)
- Affected IBM Part Numbers
- Reason for change
- Impact on Quality or Reliability commitments / performance
- Qualification data ([For semiconductor components see JESD-69](#))
- Supplier Audit results
- Reference to Advance Notice PCN notice (if applicable)
- Supplier PCN Notice

The Supplier shall make reasonable efforts to have any corrective actions in place at the time of the Execute PCN submission (e.g. Audit, quality problem, Supplier issue etc.).

5.2 Advance Notice PCNs:

Advance Notice PCNs are for awareness / planning purposes and there are no formal minimum requirements for advance notification of this planned process change.

The following non proprietary information data should be included for Advance Notice PCNs:

- Supplier PCN Number
- Supplier Contact Information (e.g. Contact name, phone, fax and e-mail)
- Type of PCN (see list in section [5.1](#))
- Commodity
- Date when IBM response is requested
- Supplier Name
- Sample availability date
- Qualification data availability date
- Is there a specification change? (Y/N)
- Original Supplier part numbers
- New Supplier part numbers (if applicable)
- Affected IBM Part Numbers
- Reason for change
- Anticipated impact of Quality or Reliability commitments / performance
- Supplier qualification plan
- Supplier PCN notice

5.3 Component Discontinuance (EOL - End Of Life):

Component discontinuances are sometimes called EOL PCNs.

The Supplier's ability to **discontinue a component** during the term of the applicable Purchase Agreement will be determined in accordance with the applicable Purchase Agreement. If the Purchase Agreement does **not contain component discontinuance** requirements, or there is no agreement in place, Suppliers shall conform to JESD 48 with the following exceptions:

- Supplier shall Notify IBM Procurement of all Supplier **component discontinuances**.
- Supplier shall Notify IBM if IBM or IBM's sub contractor has ever purchased the Supplier's **component**. This is an additional notification, where IBM may not be considered an "Affected Customer" per JESD 48.

The following nonproprietary data should be included with a component **discontinuance** notice:

- Supplier **discontinuance** number
- Notification date
- Affected commodity
- Last buy date (must be a minimum of 6 months after **the** notification date)
- Last ship date (must be a minimum of 6 months after the last buy date)
- Supplier name
- Supplier contact information (e.g. Contact name, phone, fax and e-mail)
- Original supplier component part numbers (see note below)
- Affected IBM component part numbers (see note below)
- Suggested replacement **component(s)**
- Suggested replacement **component(s)** manufacturer(s) (if applicable)
- The specification differences between the original component and the available replacement **component** (assuming both **components** are built by the same manufacturer)
- Information on supply availability of the original component **part number** (die, finished goods, distributors and brokers)
- Comments (e.g. Reason for **component discontinuance**, anticipated impact on quality and reliability statement for the replacement **component**, qualification plan for the replacement **component** (if applicable), etc.)

Note: The original Supplier component **part numbers** and affected IBM component **part numbers** must be tabbed or documented in an electronic spreadsheet to facilitate data base searches.

If a Third Party purchases the IBM part number, the **component discontinuance notice** shall be provided to both the Third Party and IBM.

The Supplier shall make reasonable effort to have samples of their available replacement **components** (for customer build and functional application testing) and qualification data at the time of the **component discontinuance notice** submission.

6. Acceptance of Final Product by IBM:

6.1 Date Codes:

Acceptable date codes of qualified product are directly controlled by the responsible IBM component engineer. Where no stricter date code limits have been imposed, components with date codes **older** than 2 years shall not be shipped, **with the exception of tactile switches which shall be 1 year**. Within the allowable date codes, the Supplier shall only ship product which meets the current Supplier and current IBM documented requirements. Shipment of Product outside of the IBM documented allowable date codes requires IBM written approval.

6.2 Component Marking and Labels:

1. **Components** shall be permanently and legibly marked as specified (see Section 2.2, "Precedence"). IBM requests that all marking be on the top side of the **component**, whenever possible.
2. If the **component** marking is not specified by a higher precedence document, the Supplier shall mark the **component** as follows (where possible):
 - Supplier Logo or EIA-476 source code number
 - IBM or Supplier Part Number
 - Code or codes to identify the fabrication, assembly, and final test plants (I.C.s only)
 - EIA-476 or EIAJ Date Code
 - Lot number if required
 - A visual indicator for pin 1 where needed
3. **Components** too small to accommodate the above marking shall be marked with Supplier standard marking.
4. Country of Origin (CoO) shall be marked on the **component** per C-S 1-1121-003, "Information Plates and Labels". **Although IBM C-S 1-1121-003 is written for IBM Products, it also outlines IBM requirements for procured components.**
5. **Components** too small to be legibly marked need not be marked.
6. Where adhesive labels are used for marking, they must withstand card assembly processing including **aqueous** and or solvent cleaning without loss of adhesion or legibility.
7. All **components** shall conform to the requirements of JESD22-B107. **Mark legibility shall be performed per JESD22-B114.**

6.2.1 Component Copyright Marking, Maskwork Protection:

1. Where IBM copyright marking is required, modules shall be marked "(c) IBM XXXX" where XXXX is the year the code was copyrighted.
2. Where Maskwork protection is required, modules shall be marked circled M "IBM" or "*M* IBM".
3. Chip metal, and each metal (where possible) level of the chip containing an IBM design, as well as the top of the package, shall be mask protection marked.
4. Where joint copyright and mask work protection is required, **components** shall be marked (c) IBM XXXX *M*.

6.3 External Dimension and Visual:

These requirements apply to all components. See Section 6.14 for requirements for modules (card assemblies).

1. The Supplier shall meet the physical outline requirements in the order of precedence outlined in Section 2.2 "Precedence".
2. For external visual requirements, all components shall meet the requirements of JESD22-B101. Components which are not ESD sensitive are not required to follow the ESD Sensitive Guidelines in JESD22-B101.

6.4 Terminal, Lead, and Ball Requirements:

6.4.1 General Solderable Finish Requirements:

These requirements apply to all components that are soldered.

1. Solderable plating thicknesses are as follows based on the plating process:
 - A. Electroplated: The plating thickness of tin (Sn) and tin alloys shall be 5-25 microns (197–984 μ -in). The preferred plating thickness for tin (Sn) or tin alloys on packages utilizing a lead frame is 7.5 microns (295 μ -in). The plating thickness of Type A Gold shall be less than 90 micro-inches (2.23 microns).
 - B. Barrel Plated: The plating thickness of tin (Sn) and tin alloys shall be 3-12 microns (120–480 μ -in), except for chip packages 0201 and smaller where the minimum shall be 2 microns (80 μ -in) . The plating thickness of Type A Gold shall be less than 90 micro-inches (2.23 microns).
 - C. Preplated: The plating thicknesses of nickel/palladium/gold (NiPdAu) preplated alloys shall meet the requirements specified by the Supplier.
2. No exposed silver (Ag) is permitted on component leads or at component lead exits.
3. Chip component (i.e. chip resistors, chip capacitors, ferrite beads etc.) shall have a 1 micron (40 μ -in) minimum nickel barrier under the solderable finish and over precious metal terminations.
4. For components not referencing IBM RoHS specifications 26P0381 or 77P0594, the solderable lead finish shall be tin-lead (Sn-Pb) solder dip, tin-lead (SnPb) alloy electroplate or one of the acceptable finishes outlined in section 6.4.2.
5. For BGA components referencing IBM RoHS specification 26P0381, the ball material must be an IBM approved tin-silver-copper (SnAgCu), tin-silver (SnAg) or a tin-copper (SnCu) alloy.

IBM prefers SAC alloys with silver concentrations of 2.5% or greater. IBM must be notified during Supplier's component qualification of the use of SAC alloys for BGA balls that have concentrations of silver less than 2.5%. This includes, but is not limited to the following alloys: SAC101, SAC105, and SAC125.

For BGA components referencing IBM RoHS specification 77P0594, the ball material must be one of the following: Eutectic tin-lead (Sn-Pb); Tin-lead-silver [(Sn(62%)Pb(36%)Ag(2%)); Tin-lead [Sn(10%)Pb(90%)].

6.4.2 Lead(Pb)-free Solderable Finish Requirements:

For components requiring a lead(Pb)-free finish, by referencing IBM specifications 26P0381 or 77P0594, the following are the only acceptable lead(Pb)-free finishes (all percentages calculated from the component solderable finish weight):

- A. Palladium-Nickel (Pd-Ni) with or without a gold (Au) flash
- B. Fused, reflowed or hot dip of 100% tin (Sn) or tin (Sn) alloys, where the alloy elements can be: Silver (Ag); Bismuth (Bi); Copper (Cu); Zinc (Zn); Nickel (Ni).
- C. 100% matte tin (Sn):
 - 1. Over 1 micron minimum Nickel (Ni).
 - 2. Over Copper (Cu) annealed at 150°C for a minimum of 1 hour within 2 weeks (24 hours preferred) of the tin (Sn) plating, where the lead pitch < 1mm (40 mils).
 - 3. Over Alloy 42 (Fe-Ni) base metal, with or without copper (Cu) underlay and anneal is not required.
 - 4. With no anneal or underplate for lead pitches > or = 1mm (40 mils).
- D. Noble metal plating is acceptable except for silver (Ag).
- E. Tin-Bismuth (SnBi) plating over copper (Cu), Nickel (Ni) or Alloy 42 (FeNi):
 - 1. With a nominal bismuth (Bi) concentration of 2-4%.
 - 2. With a total bismuth (Bi) concentration range of 1-6%.
- F. Tin - Copper (SnCu) over copper with anneal (at 150°C for a minimum of 1 hour within 2 weeks (24 hours preferred) of the tin (Sn) plating or over 1 micron (40 μ-in) minimum Nickel (Ni)
- G. Tin - Silver (SnAg) over copper (Cu) or Alloy 42 (FeNi) with a minimum silver (Ag) concentration of 1%.

Zinc (Zn) plating is not allowed as a final solderable finish or metal package final coating.

The following solderable finishes are acceptable in addition to those listed above.

Commodity	Lead Material	Solderable Finish	Solderable Finish Under plate and Minimum Thickness	Smallest Lead Pitch
Aluminum Capacitors	Cu or Fe	Sn(99.5%)Bi(0.5%)	N/A	1mm (40 mils)
Tantalum Niobium & Niobium Oxide Capacitors	Cu	SnCu	Ni[0.5 micron (20 μ-in)]	1mm (40 mils)
Actives	Cu	SnAg	N/A	0.87mm 1mm (34 mils)
Crystal / Oscillators	Alloy42	Sn(97%)Cu(3%)	N/A	1mm (40 mils)
	Alloy42	Sn(93%)Cu(7%)	N/A	1mm (40 mils)
	Alloy42	Sn(99.3%)Cu(0.7%)	N/A	1mm (40 mils)
	Kovar	Sn(100%)	Cu[2 micron (80 μ-in)]	0.75mm (30 mils)
Magnetics	Cu(94%)Sn(6%)	Sn(95%-99.5%)Cu(0.5%-5%)	Ni[1micron (40 μ-in)]	1mm (40 mils)
	Cu(94%)Sn(6%)	Sn(95%-99.5%)Cu(0.5%-5%)	Ag	1mm (40 mils)
	Cu98%Sn(2%)	Sn(95%-99.5%)Cu(0.5%-5%)	N/A	1mm (40 mils)

Magnetics	Cu or Cu Alloy	Sn(95%-99.5%)Cu(0.5%-5%)	N/A	1mm (40 mils)
	Fe(70%)Cu(30%)	Sn(95%-99.5%)Cu(0.5%-5%)	N/A	1mm (40 mils)
	Ceramic	PdPtAg	N/A	1mm (40 mils)

6.4.3 Socketed Component Finish:

These requirements apply to all components and assemblies that are socketed.

6.4.3.1 Pinned/Leaded Components:

Component pin/lead finish shall be 2.54 microns (100 mils) minimum Class A Gold over 2.54 um microns (100 mils) Nickel.

6.4.3.2 Edge Connector Contact Pads on PWBs:

Copper contact pad finish shall be 30 μ-in (0.75 micron) minimum Gold over 75 μ-in (1.9 micron) minimum of Nickel.

6.4.4 Solderability:

This requirement applies to all components that are soldered. IBM requires that all (non-BGA) RoHS Compliant components be solderable with both lead(Pb)-free, SnAgCu (SAC), and leaded(Pb) solders.

6.4.4.1 Solderability for Lead(Pb) Finishes:

This requirement also applies to BGAs with tin-lead [Sn(10%)Pb(90%)] solder balls.

1. Components shall conform to the solderability requirements of J-STD-002, per Test A, B, C or S as appropriate, for tin-lead (Sn-Pb) solder only.
2. Resistors shall conform to Steam Age Category 1 per J-STD-002.
3. Solderable Gold and preplated Palladium (including NiPd and NiPdAu) leaded components shall conform to Steam Age Category 2 per J-STD-002.
4. All other components shall conform to Steam Age Category 3 per J-STD-002.

6.4.4.2 Solderability for Lead(Pb)-free Finishes:

1. Components shall conform to the solderability requirements of EIA/IPC J-STD-002, per Test A, B, C or S and A1, B1, C1 or S1 as appropriate for both tin-lead (SnPb) and lead(Pb)-free solders.
2. Resistors shall conform to Steam Age Category 1 per J-STD-002.
3. Solderable Gold and preplated Palladium (including NiPd and NiPdAu) leaded components shall conform to Steam Age Category 2 per J-STD-002.
4. All other components shall conform to Steam Age Category 3 per J-STD-002.

6.4.5 Lead Integrity:

1. This requirement applies to all SMT and PTH components with leads and to pinned Memory modules. They shall conform to the requirements of JESD22-B105 with the following additional requirements: For test Condition A (Tension) the tensile load shall be 1.36, +0.23, -0 Kg (3, +0.5, -0 lbs) for PTH components; For test conditions B and D, an additional failure criteria shall be no flaking of the lead finish under the specified magnification.
2. Active and Passive PTH components shall conform to EIA 186-6, where the test load shall be that supported by the manufacturer. An additional criterion for type III, IV and V tests shall be no flaking of the lead finish under 10X magnification.

6.4.6 BGA Solder Ball Shear:

Applies to all ball and column grid array packages (BGA and CGA).

1. Components shall conform to the ball shear requirements of JESD22-B117, "BGA Ball Shear".
2. Test samples must be from 2 assembly lots. Sample size is 10 components per assembly lot. 10 balls per component must be sheared.
3. Test samples shall be split into 2 equal groups. One half aged for 168 hours at 125°C and remaining half shall receive no aging.
4. Minimum allowed shear values for Sn/Pb solder balls are stated in the table below: All values are average minus 3 sigma.

Solder Ball Pitch	Minimum allowed shear force for both with and without aging
≥ 1.27mm (50 μ-in)	600 grams
>1.27 mm (50 μ-in) and ≥ 1.0mm (40 μ-in)	350 grams
>1.0mm (40 μ-in) and ≥ 0.8mm (31 μ-in)	225 grams
≥ 0.5mm (20 μ-in)	80 grams

5. For lead(Pb)-free solder balls supplier must inform IBM if the shear values are below those stated in the table above for SnPb balls.
6. High speed ball shear testing per JESD22B-117 may be performed in lieu of standard (low speed) shear testing with prior written approval of IBM. High speed testing rate is 0.01 to 1.0 m/sec. Low speed testing rate is typically performed at 100 to 800 microns/second.

6.4.7 BGA Solder Ball Pull:

BGA and CGA packages shall meet JESD22-B115. With prior written approval of IBM, a supplier may substitute BGA solder ball shear data (see section 6.4.6) with solder ball pull data per JESD22-B115. Acceptance criteria will be mutually agreed to as part of the written approval.

6.5 Soldering Process Compatibility:

1. For components referencing IBM specifications 77P0594, the components shall be compatible with the leaded(Pb) solder system requirements outlined in section 6.5.1.
2. For components referencing IBM specifications 26P0381, the components shall be compatible with the lead(Pb)-free solder system requirements outlined in section 6.5.2.

3. For components not referencing IBM specifications 26P0381 or 77P0594, the components shall be compatible with the leaded(Pb) solder system requirements outlined in section 6.5.1.

6.5.1 Leaded(Pb) Soldering Process Compatibility:

These requirements apply to components referencing IBM specification 77P0594.

6.5.1.1 Wet Reflow Shock (Moisture Sensitivity) Test for SMT Components:

1. Solid-state components shall meet the requirements of J-STD-020, at the moisture sensitivity level supported by the Supplier. The moisture soak is not required for (fine leak) hermetic SMT components.
2. Non solid-state components (e.g. Optic and Passive components) shall be evaluated and classified per J-STD-075.

6.5.1.2 Requirements for Through-Hole Components:

1. All IC components in Through-Hole packages shall meet the requirements of JESD22-B106 for lead(Pb) solder conditions, with an additional requirement is that components shall provide no delamination or crack path for process chemicals to reach any feature that can be damaged by flux, or to bridge any two features of opposite polarity. This can be demonstrated through dye penetration testing and cross-sectioning, Acoustic Microscopy, or (for Memory only) Saltwater Boil testing; or can be verified by performing reliability tests after reflow simulation (preconditioning).
2. All hybrid, passive, other components in Through-Hole packages shall be evaluated and classified per J-STD-075.
3. The allowable hand solder conditions are defined by the Supplier of the component.

6.5.1.3 Requirements for Backside-Wave soldered SMT Components :

1. Logic components specifically requested by IBM to be evaluated for the Backside-Wave attach process shall be evaluated and classified per J-STD-075 with moisture soak per J-STD-020 Level 1 and Chemical Exposure being Water Soluble Flux. This is full immersion into molten solder. Contact the appropriate IBM product engineer for failure criteria. Memory components shall not be wave soldered.
2. The following Active and Passive SMT components shall be evaluated and classified per J-STD-075:
 - Chip resistor packages 0603 and larger
 - Chip resistor and resistor-capacitor array packages with than 50 mils. (1.27mm) or greater nominal pitch
 - Ceramic chip capacitors listed in per the Table 13-2 of J-STD-075. Ceramic capacitor packages smaller than 0603 and larger than 1206 shall not be wave soldered.

6.5.2 Lead(Pb)-free Soldering Process Compatibility:

These requirements apply to components referencing IBM specification 26P0381.

6.5.2.1 Wet Reflow Shock (Moisture Sensitivity) Test for SMT Components:

1. Active, Logic and Memory components shall meet the requirements of J-STD-020, at the moisture sensitivity level supported by the Supplier. The moisture soak is not required for (fine leak) hermetic SMT components.
2. Optic and Passive components shall be evaluated and classified per J-STD-075.
3. IBM must be notified if any solid state component which is not compatible with lead(Pb)-free hot air rework per J-STD-020.

6.5.2.2 Requirements for Through-Hole Components:

1. All IC components in Through-Hole packages shall meet the requirements of JESD22-B106 for lead(Pb)-free solder conditions, with an additional requirement that components shall provide no delamination or crack path for process chemicals to reach any feature that can be damaged by flux, or to bridge any two features of opposite polarity. This can be demonstrated through dye penetration testing and cross-sectioning, Acoustic Microscopy, or (for Memory only) Saltwater Boil testing; or can be verified by performing reliability tests after reflow simulation (preconditioning).
2. All hybrid, passive, other components in Through-Hole packages shall be evaluated and classified per J-STD-075.
3. The allowable hand solder conditions are defined by the Supplier of the component.

6.5.2.3 Requirements for Backside-Wave Soldered SMT Components:

1. Logic and memory components shall not be wave soldered.
2. The following Active and Passive SMT components shall be evaluated and classified per J-STD-075:
 - Chip resistor packages 0603 and larger
 - Chip resistor and resistor-capacitor array packages with than 50 mil. (1.27mm) or greater nominal pitch
 - Ceramic chip capacitors listed in per the Table 13-2 of J-STD-075. Ceramic capacitor packages smaller than 0603 and larger than 1206 shall not be wave soldered.

6.6 Hermeticity:

This requirement applies to sealed components with an internal cavity.

1. Hermetic components shall meet the requirements of JESD22-A109, Test Condition A, 'Helium Fine Leak Test', or test Condition B, 'Radioisotope Fine Leak Test'. Upon completion of either fine leak test, components shall then be tested and meet the requirements of Test Condition C, 'Fluorocarbon Bubble Gross Leak'.
2. Non-hermetic cavity packages such as PPGA or Metal QFP shall meet the requirements of Test Condition C, 'Fluorocarbon Bubble Gross Leak', only.

6.7 Cleaning Compatibility:

Non- solid state components shall be classified per J-STD-075 for cleaning compatibility. Solid state components shall be classified per J-STD-075 for aqueous cleaning processes only.

6.8 Temperature Cycling / Thermal Shock for Shipping:

Components shall withstand JESD22-A104, Condition B, 10 cycles. MIL-STD-883 method 1010 condition B , or MIL-STD-202 method 107 condition B (with low temperature as -55C) for 10 cycles are equivalent test methods and may be used in lieu of JESD22-A104, except as noted below:

Commodity	Temperature (maximum)	Temperature (minimum)
Aluminum Capacitors	(Maximum Supplier component rated usage temperature)	(Minimum Supplier component rated usage temperature)
Can/Coin Type Electric Double Layer Carbon – Special Capacitors	(Maximum Supplier component rated usage temperature)	(Minimum Supplier component rated usage temperature)
LEDs	75°C	(Minimum Supplier component rated usage temperature)

6.9 Flammability:

1. Components with volume less than 2500 mm³ (0.15³ in) shall meet UL 1694. All other components shall meet the requirements of UL 94V-0, where the test specimen shall be the component.
2. For all module (card assemblies), the assembly shall meet the Flammability requirements for "commercial components" as stated in C-S 3-0501-070.

6.10 Mechanical Shock and Vibration:

This requirement applies to hermetic and non-hermetic cavity packaged components.

Components shall meet the requirements of JESD22-B104 for Mechanical shock, at the condition supported by the Supplier, and JESD22-B103 for vibration. MIL-STD-883 method 2002 condition B or higher, and MIL-STD-202 method 213 condition F are equivalent for shock. MIL-STD-883 Method 2007 conditions A, B, or C or MIL-STD-202 method 204 condition B or higher, and IEC 60068-2-6 are equivalent test methods for vibration.

6.11 Resistance to Board Bending:

SMT ceramic capacitors shall comply with JIS-C-5101-1 section 4.35. SMT resistors shall comply with JIS-C-5201-1 section 4.33.

6.12 Insulation Resistance:

This requirement applies to components designed for use in applications over 24 volts.

1. Components shall meet the requirements of EIA RS-186-13, 100 V.
2. Electrode configuration and leakage limits shall be defined in the part number drawing.

6.13 Environmental Requirements:

- Components shall meet the requirements of IBM corporate environmental specification 46G3772. Additional IBM Environmental information can be found at:

<http://www-03.ibm.com/procurement/proweb.nsf/ContentDocsByTitle/United+States~Information+for+suppliers>

- Suppliers shall report environmental compliance per IBM PCD form part number 46C3484.
- The following exceptions to the Restriction on Hazardous Substances (RoHS) requirements are cited below per the EU Directive and subsequent amendments, at the time of this document publication. These are listed for convenience. Suppliers shall comply with the actual exemptions in affect. The prohibition is in place for all other applications. The numbering scheme below reflects the numbering of the exemptions as listed by the RoHS Directive and amendments. IBM has determined some of the exemptions will not be allowed for IBM products. This information is noted by the number.

1. Mercury (Hg) in compact fluorescent lamps not exceeding 5 mg per lamp.
2. Mercury in straight fluorescent lamps for general purposes not exceeding:
 - a. Halophosphate 10mg
 - b. Triphosphate with normal lifetime 5mg
 - c. Triphosphate with long lifetime 8mg
3. Mercury in straight fluorescent lamps for special purposes.
4. Mercury in other lamps not specifically mentioned in the Annex to the RoHS Directive 2002/95/EC.
5. Lead (Pb) in the glass of cathode ray tubes, electronic components, and fluorescent tubes.
6. Lead (Pb) as an alloying element in steel containing up to 0.35% lead(Pb) by weight, aluminum containing up to 0.4% lead(Pb) by weight, and as a copper alloy containing up to 4% lead(Pb) by weight.
7.
 - a.) Lead (Pb) in high melting temperature type solders (i.e. lead(Pb)-based alloys containing 85% by weight or more lead(Pb)).
 - b.) Note: this RoHS exemption in solder for servers, storage and storage array systems is not allowed for Deliverables referencing this specification
 - c.) Lead (Pb) in electronic ceramic parts (e.g., piezoelectronic devices).
8. Cadmium and its compounds in electrical contacts and cadmium plating except for applications banned under EU Directive 91/338/EEC amending EU Directive 76/769/EEC relating to restrictions on the marketing and use of certain dangerous substances and preparations.
9. Hexavalent chromium as an anticorrosion of the carbon steel cooling system in absorption refrigerators.
10.
 - a.) Note: the RoHS Exemption for deca BDE is not allowed for IBM Deliverables
 - b.) Lead (Pb) in lead(Pb)-bronze bearing shells and bushes.
11. Lead (Pb) used in compliant pin connector systems.
12. Lead (Pb) as a coating material for the thermal conduction module c-ring.
13. Lead (Pb) and cadmium (Cd) in optical and filter glass.
14. Lead (Pb) in solders consisting of more than two elements for the connection between the pins and the package of microprocessors with a lead(Pb) content of more than 80% and less than 85% by weight.
15. Lead (Pb) in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit Flip Chip packages.
16. Lead (Pb) in linear incandescent lamps with silicate coated tubes.
17. Lead(Pb) halide as radiant agent in High Intensity Discharge (HID) lamps used for professional reprography applications.
18. Lead (Pb) as activator in the fluorescent powder (1% lead(Pb) by weight or less) of discharge lamps when used as sun tanning lamps containing phosphors such as BSP (BaSi2O5:Pb) as well as when used as specialty lamps for diazo-printing reprography, lithography, insect traps, photochemical and curing processes containing phosphors such as SMS ((Sr,Ba)2MgSi2O7:Pb).
19. Lead (Pb) with PbBiSn-Hg and PbInSn-Hg in specific compositions as main amalgam and with PSn-Hg as auxiliary amalgam in very compact Energy Saving Lamps (ESL).
20. Lead(Pb) oxide in glass used for bonding front and rear substrates of flat fluorescent lamps used for Liquid Crystal Displays (LCD).
21. Lead (Pb) and Cadmium (Cd) in printing inks for the application of enamels on borosilicate glass.
22. Lead(Pb) as impurity in RIG (rare earth iron garnet) Faraday rotators used for fibre optic communications systems.
23. Lead(Pb) in finishes of fine pitch components other than connectors with a pitch of 0.65 mm or less with NiFe lead frames and lead(Pb) in finishes of fine pitch components other than connectors with a pitch of 0.65 mm or less with copper lead frames.
24. Lead (Pb) in solders for the soldering to machined through hole discoidal and planar array ceramic multilayer capacitors.
25. Lead oxide in plasma display panels (PDP) and surface conduction electron emitter displays (SED) used in structural elements; notably in the front and rear glass dielectric layer, the bus electrode, the black stripe, the address electrode, the barrier ribs, the seal frit and frit ring as well as in print pastes.
26. Lead oxide in the glass envelope of Black Light Blue (BLB) lamps.
27. Lead(Pb) alloys as solder for transducers used in high-powered (designated to operate for several hours at acoustic power levels of 125 dB SPL and above loudspeakers.)
28. This RoHS exemption was not allowed for IBM Deliverables and this exemption expired on July 1 2007.
29. Lead(Pb) bound in crystal glass as defined in Annex I (Categories 1, 2, 3 and 4) of Council Directive 69/493/EEC.

Batteries are exempt from the EU RoHS Directive but have their own requirements for material restrictions in other EU Directives and legal requirements in other jurisdictions. See IBM Engineering Specification 46G3772 for material restrictions for batteries.

6.14 Module Requirements:

This section applies to AOP, Logic, Memory and Power small card assemblies that are socketed or soldered to a larger planar / motherboard. Some examples are: DIMMs, memory cards, Board Mounted Power assemblies and Fiber Optic Modules.

Raw cards (PWBs) with an immersion silver finish shall not be used without IBM written approval.

6.14.1 Module Final Assembly Visual Requirements (Component, Laminate, Solder Joint, etc.):

Card assemblies shall be inspected to and meet the requirements of J-STD-001 and IPC-A-610, Class 2.

6.14.2 Module Cleanliness Requirements for Water Wash:

Per J-STD-001, Class 2, card assemblies shall have a cleanliness designator of C-22 and IBM requires that the surface contamination shall be less than 1.56 micrograms/cm² NaCl equivalent ionic or ionizable flux residue.

6.14.3 Module Gold Connector Tab Contact Requirements:

Gold plated tabs shall be inspected to and meet the "Printed Contacts" requirements of the IPC-A-600, Class 2, including plating adhesion.

6.14.4 Module Raw Card Requirements:

6.14.4.1 Module Raw Card Solderable Finish Requirements:

Except for the specific exemptions listed in section 6.13, printed circuit boards must not contain lead(Pb) in amounts greater than those shown in Table 1 of IBM specification 46G 3772., including printed circuit board finishes. The RoHS-compatible finishes listed in Table 3 must also pass further IBM standard qualifications outside the scope of this specification. The acceptable raw card finishes are as follows:

Finish	Notes
Immersion Tin	Requires approval from IBM Procurement Engineering
Organic Solder Preservatives (OSPs)	Preferred, for example benzotriazole (BTA). Refer to IBM Procurement Specification 53P4082 for guidelines in selecting the appropriate OSP.
HASL (Hot Air Solder Leveled) Tin or Tin Alloy	Requires approval from IBM Procurement Engineering
Immersion Silver	Requires approval from IBM Procurement Engineering
Electroless Nickel Immersion Gold	Requires approval from IBM Procurement Engineering
Electrolytic Nickel with noble metal over plate	Requires approval from IBM Procurement Engineering

6.14.4.2 Module Raw Card Solder Process Compatibility Requirements:

The raw card / laminate material must be compatible with leaded(Pb) and Lead(Pb)-free assembly process. The surface finish must be compatible with the Lead(Pb)-free solder alloys. Note that other IBM specifications may be applicable to the qualification of a PCB IBM Engineering Specification Supplier's use of any surface finish on a PCB used for IBM. Contact IBM PCB Procurement Engineering for further information.

6.14.5 Custom DIMM Raw Card Requirements and Recommendations:

6.14.5.1 Qualification and AVL Control:

It is DIMM suppliers' responsibility to determine if a raw card (PWB/PCB) Supplier has capability to manufacture the raw card for a specific IBM custom DIMM. For each manufacturing site of the raw card, DIMM Suppliers shall maintain an AVL that reflects the complexity of raw card technology and material set. See Appendix B for the mandatory raw card/AVL attributes and sample tracking spreadsheet.

6.14.5.2 Traceability:

Raw card serial number, panel number, lot code, date code and week code are identifiers that are recorded and can be correlated to each definable stage within the raw card Supplier's process.

IBM customer DIMM suppliers shall establish minimum printed raw card traceability. Panel-level traceability is strongly recommended. Backward traceability level and bounding capability to each definable raw card process stage shall be documented by custom DIMM Suppliers and provide to IBM upon request.

6.14.5.3 Early Manufacturing Ramp-up:

Suppliers shall submit First Article Inspection (FAI) samples from the raw card Supplier for all custom DIMM part numbers, for IBM's review and approval. All new raw card technology requires IBM FAI and approval.

IBM recommends Supplier Readiness Reviews for new custom DIMM technology. See Appendix C for IBM's suggested custom DIMM SRR agenda/topics.

6.14.5.4 Ongoing Quality and Reliability Monitoring:

Custom DIMM Supplier's shall:

- Perform 100% visual inspection on the incoming raw card. Visual inspection shall include: the outline specification; plated through holes; solder web; gold tab; and overall workmanship.
- Submit to IBM a bi-weekly assembly yield reports with disposition from DIMM suppliers, and a monthly report of failure analysis/pareto of failures chart for PCB induced assembly pull.
- Establish in-process and on-going quality/reliability monitoring programs with their raw card Suppliers, consistent with the requirements of this specification. IBM Custom DIMM Supplier's shall use the format in Appendix D to document their manufacturing and quality/ reliability processes controls/monitors. IBM approval is required of all Supplier in-process control and quality reliability monitoring programs.

6.14.5.5 MPE Program:

All IBM custom DIMM Suppliers shall:

- Have an active MPE program consistent with section 4.2. The intention of this program is the minimization/elimination of: low yielding manufacturing lots; reworked product; or any manufacturing material/component/module requiring MRB intervention/action.
- Process Variation Anomalies: The raw card Suppliers shall have detailed procedures managing process anomalies at each process stage. These procedures shall specify process anomalies that require escalation and material quarantine.
- Yield Clip Limits: DIMM Suppliers shall require that their raw card Suppliers shall have documented yield clip limits in place for disposition. These limits shall be established as part of the process/technology qualification process. This information shall be provided to IBM upon request.
- Material Review Board (MRB): DIMM Suppliers shall require that their raw card Suppliers implement an MRB to review and determine the disposition of nonconforming material. Nonconforming raw card material shall not be shipped without prior notification and approval from the DIMM suppliers and IBM.

6.14.5.6 Continuous Improvement:

DIMM Suppliers shall require raw card Suppliers to continuously improve their products and services per section 8.2.

6.14.5.7 Audits:

DIMM Suppliers shall have an on-going quality audit program for each of their raw card Suppliers and shall perform a quality audit at least once a year of all their custom DIMM raw cards.

6.14.5.8 DIMM Supplier's Raw Card Supplier SQR:

DIMM Supplier's shall have SQR type meetings with their raw card Suppliers where the raw card is not meeting the DIMM Supplier's requirements. The SQR should cover the information outlined in section 8.3 and Appendix D.

6.14.6 Module DIMM Torque Requirements:

DIMMs shall be capable of being torqued 1.8° per inch length of the DIMM for 25 cycles. The maximum torque frequency is 0.5 Hertz.

All visible solder joints on the DIMM shall be inspected before and after the test. Any cracking shall be noted.

No fracture of the solder joints after test in excess of 25% of the fillet length is allowed when viewed at 10X magnification.

The DIMM should be verified to be electrically functional at 0°C, 25°C and 70°C before and after the test.

6.14.7 Additional DIMM Requirements:

DIMMs shall be compliant with IBM specification 77P3021.

6.15 Components with Batteries:

These requirements apply to all components, modules, and subassemblies that contain a battery (this includes 'button cells').

1. All components, modules, and subassemblies must meet the content and labeling requirements of IBM specification 46G3772, section 2.5, and IBM specification 92F6933.
2. Information regarding the battery chemistry must be provided to IBM during the qualification of the component, module, or subassembly.

6.16 Components with Pluggable Connectors:

Components with non-fiber optic pluggable connectors shall have a gold plated pluggable contact finish of 50 μ -in (1.27 microns) minimum over nickel, or an IBM approved equivalent finish

6.17 Shipping and Packing:

6.17.1 Component Packing and Labeling:

1. The original manufacturer's label shall remain visible on first and interim level containers whenever possible.
2. All levels of containers and **packing** materials shall not adversely affect the functionality, quality and reliability of the component.
3. Shipping requirements and labeling of shipping containers shall be specified by the ordering location where not in conflict with this specification.

6.17.2 Shipping Container:

This container contains multiples of interim level containers and / or multiple first level containers. This container may have multiple IBM part numbers and or IBM purchase order numbers (e.g.. Such as a consolidated shipment).

6.17.3 Shipping Container Label:

When a shipment consists of multiple part numbers and or purchase orders (that is, a consolidated shipment) the appropriate label field(s) shall be marked "MULT", including the Date Code and Quantity fields. All consolidated shipping containers must have interim containers. The contents of a consolidated shipment shall not be divided between multiple shipping containers.

6.17.4 Interim Container:

This package level contains multiples of first-level containers. This container must be of the same IBM part number and purchase order number.

6.17.5 Interim Container Label:

The interim container label requirements are the same as the shipping container label.

6.17.6 First-Level Container:

This package level contains multiples of the individual electronic components. Components are of the same IBM part number. Examples of these containers are: Tape and Reel (pizza box), Tubes, Tube boxes (bags), Tray stacks, Ammo boxes, etc.

6.17.7 First-Level Container Label:

Labels shall be placed on all component containers (e.g. Tape & reels, tubes or tube boxes, ammo boxes, reel, tube or tray stack dry packs, or bags), with the exception of tubed product with less than 100 components.

Label Placement:

- Tube labels (required where more than 100 **components** are in each tube) shall be placed on the tube surface opposite **component** lead tips near the lengthwise center of the tube, per Section Item. Labels may wrap around the sides provided they are readable.
- Tube box labels shall be placed on the box front.
- Reel labels shall be placed on or as close to the reel flange as possible, on the reel face opposite the tape round sprocket holes.
- Ammo Box labels shall be located per EIA 468.
- Tray stack labels shall be on the ESD / dry bag. If no bag is used, the label shall be placed on the next level container.
- Dry Packed **components** shall have a label on the dry pack.
- If the inner component container is not labeled at dry packing, a second peelable label shall be placed on the dry pack.
- If the first-level container is shipped in a bag or box, where the label is not viewable on the first-level container through the bag or box, the bag or box containing the first-level container must also be marked with a copy of the label.
- See section [6.16.9](#) for moisture sensitive label requirements.

A maximum of two date codes are permitted per component first level container. Multiple lot codes per first level container carrier are acceptable. In this situation, the date code on the first level container shall be the one with the greatest number of parts in the container.

The first-level container label shall have the following human readable machine generated label information:

- Customer Part Number (e.g.. IBM Part Number)
- Supplier Name
- Quantity
- Date Code
- Country of Origin (per IBM C-S 1-1121-003). [\[Although IBM C-S 1-1121-003 is written for IBM Products, it also outlines IBM requirements for procured components.\]](#)

The following additional information is preferred, but not required:

- Lot Code
- Supplier Part Number

Bar coding requirements of the first-level container label information is optional. Bar coding may be specified by the ordering location, but the bar code label must include or not cover-up the human readable data requirements outlined in this section.

6.17.8 Electrostatic Discharge (ESD) Control Requirements and ESD Sensitivity:

These requirements apply to all shipments of [components](#) characterized as ESD sensitive.

1. [Components](#) shall be characterized according to the JESD22-A114, "Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)", and JESD22-C101, Field Induced Charged Device Model (CDM). [This information shall be provided to IBM by the Supplier during the Supplier's qualification or re-qualification.](#)
2. All shipments shall meet JESD 625.

6.17.9 Moisture Sensitive Component Packing for Shipping and Handling:

This applies to [components](#) classified by their manufacturer as moisture sensitive per J-STD-020.

1. Moisture sensitive [components](#) must conform to the requirements of J-STD-033 for Supplier [packing](#) and labeling. [For polymer technology capacitors, where the classic "popcorn" effect defect mechanism does not exist, color changing silica gel may be used in place of the HIC card.](#)
2. All moisture level 6 components shall be marked with the word "bake".
3. Moisture sensitive [components](#) shall have a minimum of 6 months before expiration of the desiccant at the time of shipment. This does not apply to components which are classified as moisture sensitivity levels 1, 2 and 6.
4. Cardboard boxes shall not be enclosed inside the moisture barrier bag.

6.17.10 Process Sensitive Component Packing and Labeling:

This applies to [components](#) classified by their manufacturer as process sensitive per J-STD-075.

1. [Process sensitive components](#) shall be labeled and packed per J-STD-075

6.17.11 Tape and Reel Requirements for Surface Mount Components:

1. All surface mount [components](#) shipped to IBM must be packaged in tape and reel according to the requirements of EIA 481, with the following exceptions:
 - Quad flat packs of greater than 14 mm square body size and PGA's of greater than 27 mm square body size shall use trays.
 - Blank programmable logic and memory [components](#) shall use tubes, trays or tape and reel. Tape and reel only is allowed where [component](#) programming is occurring after card assembly.
 - [Components](#) requiring a bake before assembly shall use bakeable trays with a minimum rating of 125deg.C.

2. If a component can be placed in multiple pocket pitches or widths, the Supplier shall request IBM approval for the Supplier suggested pocket pitch and width before an initial shipment is made. In addition Supplier shall request IBM approval for changes to a parts existing pocket pitch and width, using the Process Change Notice (PCN) process.

6.17.12 Tape and Reel Requirements for Radial and Axial Lead Components:

1. **Part numbers referencing these replaced specifications:** 6496427, 82G6730 or 6188635, shall be packaged in ammo boxes.
Part numbers referencing these replaced specifications: 57G8318 or 2412436, shall be packaged in reels.
2. Radial components in both tape reel and ammo box shall comply with EIA 468.
3. Axial Lead components shall comply with EIA-296.

6.17.13 Tray Packing Requirements For PTH and SMT Modules:

These requirements apply to BGA's (too large for tape and reel), QFP's of body size greater than 14 mm, PGA's unless tubes are called out in the part number drawing, and any component requiring a customer bake before assembly.

1. PGAs shall be packaged in JEP 95 CO-010 trays. Quad Flat Packs shall be packaged in Appropriate JEP 95 or EIAJ thin (6.35 mm nominal stacked thickness) matrix trays.
2. Trays shall be injection molded.
3. All SMT modules shall be captive in the tray cavities such that the terminal leads or BGA balls do not contact the tray during shipping and handling.
4. Pin one of each component shall point towards the tray chamfer. Trays shall be stacked each with the chamfer in the same orientation.
5. Tray stacks shall be no more than 12 high.
6. Trays shall be bound together with plastic straps. Rubber bands are not allowed. Velcro straps are allowed for PTH components only.
7. Components classified as level 5 or 6 per of J-STD-020 shall be packaged in 125° C minimum temperature rated bakeable trays, which must be electrostatically dissipative per EIA-541.

6.17.14 Slide Tube Packing Requirements:

These requirements apply to all components shipped in tubes.

1. PGA's shall be shipped in tubes only where the replaced specification 6413033 is referenced on the part number drawing. Otherwise use trays.
2. Modules shall be oriented in the same direction in tubes. Orientation shall not vary from tube to tube or lot to lot.
4. Tube or slide pack material shall be transparent or have a transparent window so that module orientation and marking can be seen.

5. Modules shall slide freely in tubes.
6. Tube closure shall be mechanical, no tape is allowed.
7. When loading ceramic or other hermetic modules in tubes, tilt shall be 30 degrees or less from horizontal.
8. Modules shall not be allowed to move in closed tubes. PLCC's shall not be placed in compression by the tube closure.
9. Tubes of ceramic and other hermetic modules such as oscillators shall have the module column placed in compression by an electrometric closure.

6.17.15 Bulk Packing Requirements:

These requirements apply to any bulk shipment. Where IBM does not specify second level [packing](#), use [the](#) above industry standard auto insertable methods. Where IBM specifies bulk [packing](#), or Suppliers cannot supply autoinsertable product, the following requirements must be met:

1. [Components](#) shall be placed in a clear poly-type bags, either "zip lock", heat sealed, or closed with two or less staples.
3. Bags shall be placed in corrugated cardboard boxes with suitable filler to separate bags, protect [components](#), and stop movement.
3. Where practical, full bag quantities shall vary in increments of 100.

6.17.16 Shipping Requirements For Components Used In Manual Assembly:

1. [Components](#) should be packed for manual assembly with suitable filler or additional [packing](#) levels to protect [components](#) and stop movement.

6.17.17 Bare Die and Chip Scale Package Shipping And Handling Requirements:

1. Bare Die and Chip Scale Packages shall be taped and reeled according to [EIA-763](#).
2. All product, which cannot be taped and reeled or when IBM documents that the part shall not be tape and reeled, shall be shipped in waffle packs or equivalent in sealed bags as follows:
 - a. When placed in the waffle pack pocket, the total clearance between the chip and the waffle pack side wall shall be no greater than 0.5 mm in either direction.
 - b. Maximum chip rotation allowed relative to the pocket is 5 degrees.
 - c. Waffle packs may contain an insert to prevent chipping or breakage.
 - d. Material water soluble contamination levels shall be less than 1ug/cm² NaCl equivalent.
 - e. 1 to 12 waffle packs shall be stacked and banded or boxed securely.
 - f. [Components](#) in a pack and packs in a stack shall have the same orientation.
 - g. A stack may contain only one wafer lot. All stacks of one lot must be in the same carton.

7. Stopship / Stop Build Procedures:

7.1 Failure Analysis and Corrective Action Plans:

Written corrective action is required for all returned verified component failure mechanisms. This information is a measure of quality / reliability, and is an aid for continuous improvement.

Failure analysis response times will comply with the guidelines in JESD 671 Section 6.8 or as requested by IBM. IBM identified "Box" and "Field" failures are considered "Urgent" and IBM identified "Card" failures are considered "Standard".

The Physical Failure Analysis Report shall, at a minimum, meet the requirements of JESD 38.

7.2 Quality Problem Notification:

The Supplier must notify IBM and any third party procuring the affected IBM parts number(s) of any quality or reliability problems that have been identified either by the Supplier's or Supplier's subcontractors internal testing (that is: production or reliability monitoring test data, process control data, burn-in data, etc.) or by another customer when the problem may affect IBM product. (See ISO 9001)

In case of a problem, the Supplier shall provide IBM with the requested traceability data (P/N, Lot number, Date code, Volumes, Ship to locations, etc.) within 48 hours. IBM may request a faster response on severe problems.

The notification should address an immediate containment plan and indicate a schedule for definition and implementation of permanent corrective actions per JESD 671.

Supplier shall make no shipment of suspect product to IBM or IBM's authorized subcontractors without written IBM approval. All repaired or re-screened product requires written IBM approval prior to reshipment to any ordering location.

8. Quality Goals, Continuous Improvement and Reporting:

8.1 Quality System and Program Compliance:

The Supplier shall have a Quality System and Program capable of maintaining an uninterrupted flow of product and meeting IBM's quality / reliability requirements set forth in this Specification, or as may be agreed in a separate Supplier Quality Document (SQD). The Supplier's Quality System and Program shall include documentation control, procedural control, Supplier internal certification, Supplier internal audit, and established statistical process controls which correlate with functional performance.

The Supplier shall maintain an internal certification program designed to assure the adequacy of their quality system as well as conformance to that system. To assure Environmental compliance, the Supplier shall have a comprehensive physical product composition verification / compliance process for their product(s) and their subcontractor's product(s).

The Supplier shall meet all requirements of IBM specification 03N6596, "IBM Supplier Quality Requirements Document (SQRD)".

[See Appendix D for additional IBM custom DIMM quality monitoring requirements.](#)

8.2 Continuous Improvement:

The Suppliers shall strive to continuously improve their products and services. The objective of continuous improvement is to meet or out perform the mutually agreed IBM requirements for quality and reliability. [The IBM SQR, which is sometimes included as part of the IBM BTR, shall](#) be used to evaluate Supplier’s Continuous Improvement Program.

Continuous improvements must be measurable. IBM recommends that the following “best practice” industry specifications / standards be used:

Document Number	Document Name
EIA 599	Continuous Improvement
ISO 2859	Sampling Procedures for Inspection by Attributes
ISO 3951	Sampling Procedures for Inspection by Variables
JESD 50	Special Requirements for Maverick Product Elimination and Outlier Management
JESD 659	Failure-Mechanism-Driven Reliability Monitoring

8.3 Supplier Quality Review (SQR):

Supplier agrees to use reasonable efforts to participate in Supplier Quality Review meetings, sometimes conducted as part of a Business Technical Review (BTR), with a frequency mutually agreed by the parties. If Supplier is failing to meet the committed quality levels, IBM shall have the right to request SQR meetings on a frequency consistent with the magnitude and urgency of the problem(s). At those meetings, Suppliers shall review their Quality System and Program, product performance, continuous improvement plans and related topics (listed below). (Contact your procurement engineering contact for a copy of your commodity’s SQR agenda). The following agenda items are typical for an electronic components SQR meeting:

- Review of Supplier manufacturing and subcontractor manufacturing facilities locations and addresses by product / component part family.
- Historical quality performance for all shipments of IBM part numbers and total customer base, including root cause and written corrective actions.
 - [Quality testing and monitoring](#)
- Historical reliability performance for IBM and total customer base including root cause and written corrective actions.
 - [Reliability testing and monitoring](#)
- Manufacturing process control and monitoring programs
- Maverick Product Elimination (MPE) Program
 - [Non-Conforming Material Management \(Scrap Control\)](#)
 - [Down-level part management \(where applicable\)](#)
 - [Sub-Contractor and Sub-Tier Supplier Management](#)
 - [Production Electrical Test Management](#)
- Internal audit results and corrective actions
- Current (Execute PCN) and future (Advance Notice PCN) Process Change Notifications
 - [Supplier Major vs. Minor Process Change Definitions to JESD46](#)
- Past and Future [Component Discontinuance](#) (EOL)
- Continuous improvement plans, resulting in meeting or out performing SQD quality and reliability commitments
- Methodology used to derive reliability and quality commitments
- Specification conformance to IBM and industry specifications
 - [Review of recent specification changes](#)
- Environmental compliance and reporting

- Physical verification process of content
- Content change management including Sub-Contractor and Sub-Tier Suppliers
- Reporting management
- Supplier SQD Status
 - Supplier specification exceptions
 - Quality and Reliability Commitments
 - SPEX Process Agreement
- Supplier Product and Supplier Facility Qualification Status
- Open Technical Issues
- Supplier Product and Technology Road Maps
 - Recent new Product introductions

9. Audits:

See section 6.14.4.7 for additional requirements for DIMMs.

10. Quality Records:

10.1 Statistical Process Control and Data Retention:

Suppliers must demonstrate that they have a process capable of consistently meeting this requirement. A well developed Statistical Process Control (SPC) program is necessary to achieve and demonstrate this capability. IBM recommends that the “best practice” industry specification / standard EIA 557 be used.

The SPC program for Suppliers facilities and at their respective subcontractors facilities must be broad in scope, encompassing not only the manufacturing processes and tools, but also include incoming raw materials, sub components and completed Product,. The SPC limits must be reviewed on a predetermined basis for continued adequacy and improvements, along with updates as the process capability improves.

Non-confidential Supplier SPC data (such as, raw data or control charts, CP and CPK for critical/identified process operations) shall be available for review by IBM upon request. IBM will review the Supplier's SPC data upon receipt and/or during audits to determine the level of process improvement. Supplier and their respective subcontractors shall establish and maintain procedures for identification, collection, indexing, filing, storage, maintenance, and disposition of all quality records including, but not limited to: Statistical Process Control (SPC) data for a minimum of three (3) years. Suppliers shall maintain all published data sheets (all revisions) from product initial release to three (3) years beyond the products End Of Life (EOL). Supplier and their respective subcontractors traceability data shall be retained for three years.

11. Standard Compliance Requirements:

There are no additional commodity specific requirements in addition to those stated in the SQRD (03N6596).

12. Equipment Control:

There are no additional commodity specific requirements in addition to those stated in the SQRD (03N6596).

13. Training and Workmanship:

There are no additional commodity specific requirements in addition to those stated in the SQRD (03N6596).

14. IT Toolsets:

There are no additional commodity specific requirements in addition to those stated in the SQRD (03N6596).

15. Buyers Qualification of Product:

There are no additional commodity specific requirements in addition to those stated in the SQRD (03N6596).

16. Related Documents:

Upon IBM's request, IBM and Supplier shall negotiate Supplier's specific quality and reliability commitments to IBM in a Supplier Quality Document (SQD). The SQD shall be referenced in the IBM / Supplier Agreement.

The following minimum information shall be contained in the SQD, which shall be signed by IBM and the Supplier's Quality Manager:

- Yearly (ppm) Quality commitments for the current year through the next three years.
- Yearly Reliability (failure rate in ppm/Khr.) commitments for the current year through the next three years.
- Supplier specification exceptions.

IBM may require additional quality or reliability monitoring requirements, which will be referenced in the IBM business agreement or equivalent documentation. The frequency of the SQD and subsequent signatures will vary by commodity. The IBM Procurement Engineer shall initiate initial SQD process and all subsequent updates, as required. IBM may provide an SQD template.

Appendix A: Documents Replaced By This Specification

The following IBM specifications have been replaced by this specification:

IBM Specification	Specification Title
866348	Mechanical Requirements for Surface Mount Components
871300	Electrical Components General Requirements
873443	Supplier Shipping Specifications
873506	Electrical Components General Requirements
873511	Module Package Seal Requirements
873522	Components Glass to Metal Construction
873523	Glass to Metal Package Seal Requirements
873531	Axial Lead Discrete Diode Package Mechanical Requirements
873532	Axial Lead Discrete Diode Package Seal Requirements
873540	Power Semiconductor Device Mechanical Requirements
873587	Dual Inline Module Mechanical Requirements
873589	General Requirements (Technical) for Purchased Electronic Components
873641	Mechanical and Chemical Requirements for Plastic Semiconductors
873657	Supplier Component Parts Minimums
873658	Packaging RC Form Factor Modules - SIP
873728	Power Package Mechanical Requirements
1590087	Packaging of Ceramic Dipped Capacitors
19F7472	Ceramic SPT Capacitors Mechanical Shock Test Procedure
23F0325	Packaging of Modules in Matrix Trays
23F0353	Single In-Line Package (SIP) Assembly Mechanical Requirements
23F0365	Die Handling, Shipping and Storage
2412322	Packaging of Dual Inline Modules
2412436	Packaging of Axial Leaded Components
2413138	Engineering Flammability Specification for Purchased
2413145	Packaging of Dipped Mica Capacitors
4429688	Hermetic Dual-In-Line Module Seal Requirements
42F2811	Multilayer Plastic Pin Grid Array Chip Carrier (PPGA)
42F2894	Silicon Chip Specification
4481265	Packaging SIP Type Components in Plastic Slide Tubes
55X0213	Shipping Specification, Category III
57G8318	Packaging of Radial Leaded Components
5892841	Special Handling Procedure - Mosfets
6016050	FET LSI / VLSI Anti-ESD Handling Procedure
6016060	Multi-Layer Ceramic Chip Carrier with Hermetic Seal and Brazed Area Array Terminal Leads
6188544	Category 3 Module Physical Outline Requirements
6188600	Lead Taping and Packaging of Radial Leaded Aluminum Capacitors
6188635	Packaging of Axial Leaded Components in Ammo Boxes
6231587	Mechanical Requirements for Surface Mount Components
6413033	Shipping of Pin Grid Array Modules
6413056	Electrostatic Discharge Sensitivity Measurement Procedure
6496427	Packaging Radial Leaded Components for Automatic Handling
6496700	Tape and Reel for Leadless SMT Components
68X5409	Packaging of Large Aluminum Capacitors

68X5436	Packaging Crystal Oscillators for Shipment
68X5508	Packaging Discrete Crystals for Shipment
68X5655	Moisture Sensitive Component Requirements
68X5727	Bar Code Marking Requirement for Mechanical Electrical and Electronic Carriers
71F7704	SMT Hybrid Card Assembly Requirements
74G1388	IBM Requirements for Industry Plus Parts
78G9129	Quality Requirements for Purchased Electronic Components
82G6730	Packaging of Single-In-Line Packages in Ammo Boxes
8519509	Electro-static Discharge (ESD) Control Handling Procedure
8519558	Protection Notice Marking Requirements for Personalized IC
8519913	Packaging Gold Leaded SIP Rpacks in Plastic Slide Tubes

Appendix B: IBM Custom DIMM Raw Card / AVL Minimum Data Attributes

- Raw Card Supplier Name
- Raw Card Manufacturing Location
 - City
 - Country
- IBM Design Part Number
- DRAM Supplier Design Number
- Layer Count
- CCL Core Material
 - Supplier Name
 - Part Number and Material Name
 - Type
 - Tg
- B-Stage Prepreg
 - Supplier Name
 - Part Number and Material Name
 - Type
 - Tg
- External Copper (Cu) Foil
 - Supplier Name
 - Part Number and Material Name
 - IPC Foil Profile
- Internal Copper (Cu) Foil
 - Supplier Name
 - Part Number and Material Name
 - IPC Foil Profile
- Solder Mask
 - Supplier Name
 - Part Number and Material Name
- Solderable Finish
 - Supplier Name
 - Part Number and Material Name
- External Layer Design Criteria
 - Copper (Cu) Foil Weight (oz.)
 - Minimum Trace Width and Tolerance (microns)
 - Minimum Trace Spacing and Tolerance (microns)
 - DRAM BGA Pad Types (SMD or NSMD)
 - BGA Pad Diameter and Tolerance (microns)
 - IBM custom Memory Buffer BGA Pad Types (SMD or NSMD)
 - IBM custom Memory Buffer BGA Pad Diameter and Tolerance (microns)
 - Minimum Solder Dam (mm)
- Internal Layer Design Criteria
 - Copper (Cu) Foil Weight (oz.)
 - Minimum Trace Width and Tolerance (microns)
 - Minimum Trace Spacing and Tolerance (microns)
- Via Technology
 - Minimum PTH Drill size (mm)
 - Minimum PTH Pitch (mm)
 - Minimum PTH to Pad Air Gap (mm)
 - Minimum PTH Drill size (mm)

- Sub Composite? (Yes/No)
- 1-2 Blind Via (Yes/No)
- 1-3 Blind Via (Yes/No)
- IVH (Yes/No)
- Via on Pad? (Yes/No)
- Tab Contact
 - Gold (Au) Thickness (microns)
 - Nickel (Ni) Thickness (microns)

Appendix C: IBM Recommended Custom DIMM Supplier Readiness Review (SRR) Agenda/Topics

General:

- Project Name
- Part Number
- Layer count
- Board thickness
- Minimum hole size (drill and PTH)
- Minimum line width/ spacing (inner and outer)
- Material (Type / Tg):
- How many ups per panel?
- Surface finish

Layup:

- Prepare/ core complies with IBM requirement?
- Thickness requirement?
- Manufacturability of the concerned layup?
- Resin content for high Cu content inner layers?

Impedance Requirement:

- Line width compensation (inner and outer)?
- Dielectric thickness?
- Impedance coupon and circuitry consistency?
- Impedance testing on board vs. panel coupon

Artwork:

- Manufacturability discussion
- Compensation factor for line or any other features?

Cu Plating:

- DC or pulse plating
- Panel plate/ pattern plate control parameter

Outline:

- Critical dimension/ tight tolerance manufacturability discussion

Quality Control Plan:

- Sufficient gating for Quality assurance?

Technical Data Package (Documentation/Specification):

- Available and complete?
- Issues? Waivers?
- Reply of technical questions?
- Supplier familiarity with relevant IBM Spec requirements

Coupon Requirements (IST, SF, Impedance, etc):

- On board Zo coupons in the design?

Appendix D: IBM Custom DIMM Raw Card Supplier Manufacturing Process Document

Supplier Name:
Physical Address:
Telephone Number:
Internet URL:
Audit Date:

Materials:

- a. Laminate Material - Please provide the following information for each laminate material offering.
 - 1. Supplier Name
 - 2. Material Name

- b. Solder Mask - Please provide the following information relative to each surface finish offering:
 - 1. Supplier Name
 - 2. Material name
 - 3. Method used to apply material
 - 4. In Plant or Outside Service

- d. Surface finishes - Please provide the following information relative to each surface finish offering:
 - 1. Type of Finish (OSP, ENIG, Immersion Silver, etc.)
 - 2. Supplier Name
 - 3. Material Name
 - 4. In Plant or Outside Service

PCB Parameters:

- a. Panel Sizes
- b. Lamination Type (Pin, Sequential, Buried Via Cores, Subcomposites, etc.)
- c. Drill - Identify various offerings (mechanical drill, laser drill, smart drill,)
- d. Electrical Test Parmeters - Voltage, Continuity Resistance, Isolation Resistance (Preferred and minimum continuity resistance, maximum voltage, minimum isolation resistance)
- f. Hi-Pot Testing - Standard and maximum voltage for both cores and composites
- g. Impedance Control - Single Ended, Broad Side/Edge Coupled Differential, tolerance.
- h. Warpage Control - Tolerance

Quality Assurance System

Verification of Certificates

- a. UL certification : _____
- b. ISO 9000: _____
- c. ISO 14000: _____
- d. QS 9000: _____
- e. Other certification: _____

General:

- a. Quality system in general (Mission/Objective/Organization/System)
- b. Check list control in action?
- c. Internal Audit in action?
- d. Statistical Process Control in action?
- e. Quality tools in action?

Quality Data Management System:

- a. Is electrical test yield data fed back to AOI inspection?
- b. Is electrical test and AOI defect data fed back to internal and external circuitization operations?
- c. Is incoming inspection of raw materials done? If so, how is quality data tracked and used to manage and improve material supplier quality?
- e. For subcontracted manufacturing operations are PCB's inspected both prior to leaving the plant and after arrival back in the plant?

SPQL:

- a. Is shipped product quality data collected from each customer and used to improve adequacy of quality inspection operations and process/equipment problems? Show examples of how this data is tracked and used both from a general and individual part number perspective.

SPC:

- a. List all product (dependent) variables which are tracked and controlled with SPC (e.g. copper plating thickness, impedance, trace width, panel thickness, etc.)
- b. Are product (dependent) variables controlled to a Cpk of 1.33 minimum?
- c. How often is gauge R & R done on each measurement tool in the factory? What are the minimum R & R requirements for the gauges?
- d. What techniques have been used to choose process (independent) variables that require tracking and control via SPC (e.g. FMEA, ANOVA, DOE, etc.)?
- e. Are process variables controlled to a Cpk of 1.33 minimum
- f. Are manufacturing operators able to shut down a process when SPC variables go out of control?
- g. Are trend analysis rules used to control trending of either product or process variables? Give examples of which rules are being used? Show corrective action report for poor/out of control cases.
- h. Is SPC tracking of product variables used to identify maverick lots of production PCBs? (e.g. Out of control points for X-Bar R chart, dependent variables outside of control limits, failure of unnaturalness test, etc.) If not, then what is used to identify maverick lots?
- i. Identify the type and amount of SPC training that is required by each of the various levels of personnel.

Final Inspection:

- a. What type of visual inspection aid(s) are used by quality inspectors for the final inspection operation? (e.g. microscope, dazer lamp, etc.)
- b. Are all parts final inspected 100% or is a sampling plan used? If a sampling plan is used please provide details of this sampling plan?
- c. Are gold tabs inspected 100% or according to a sampling plan? What visual aid(s) are used for this inspection?
- d. Do quality inspectors have immediate, direct access to all customer quality specifications?

Reliability Testing:

- a. Which of the following tests are performed on a regular basis, regardless of customer requirements, in order to monitor product reliability: solder float test, CAF/IR test, solderability, IST or other form of via reliability testing, gold porosity, Composite Hi-Pot?
- b. What is the frequency and sample size of this reliability testing?
- c. Identify the key test parameters used for each of these tests.
 - 1) Solder Float Test: # of floats, solder temperature, sec./float, type of polish, Sandpaper Grit for each step in the grinding process, type of potting material - curing time, type of automatic grinding and/or polishing equipment, hole diameter, number of holes per sample. Are coupons fluxed only prior to the first float or before each float? Are the coupons flipped between each float? What temperature and time are used for pre-bake of the coupons prior to solder float? What is the pass/fail criteria used?
 - 2) CAF/IR test: temperature, humidity, voltage, number of hours, failure criteria.
 - 3) Solderability: IPC test procedure? pre-conditioning procedures?
 - 4) IST: temperature, coupon design, number of cycles, pre-conditioning steps, via sizes and aspect ratios, number of vias.
 - 5) Gold Porosity: Test type (bulk gel medium, nitric acid, etc.)

6) Composity Hi-Pot: voltage, ramp rate, dwell time

Manufacturing Process:

Front End Engineering

- a. Is a checklist used to verify completion of all work prior to release of a new p/n to the manufacturing floor? Show a copy of the checklist. Review the receiving procedure of the gerber data.
- b. Is a netlist generated from the gerber data and compared to the netlist supplied by the customer?
- c. Are customer design specifications used as a part of the design rule check?
- d. Are design rule violations and manufacturability problems reported back to the customer for each new part number?
- e. When design or drawing or specification questions are uncovered that require customer response how does this impact the turn around time or delivery date?

Artwork Generation:

- a. What brand, model of photo plotting equipment is in use?
- b. What type of film is in use (e.g. Silver Halide, Diazo, or glass)?
- c. Resolution of photo plotting equipment (e.g. 1/4 mil, 1/8 mil, 1/16 mil)?
- d. Is artwork stored in clean area in temperature and humidity controlled conditions?
- e. Is temperature humidity control tracked by chart recorder? If so, does the chart recorder sound off an alarm for out of control conditions? Is the chart paper regularly checked and changed?
- f. % utilization of photoplotting equipment?
- g. Is first generation artwork always used?
- h. Is AOI of phototools used?
- i. How often is the positional accuracy and dimensional accuracy of the plotter checked? What tools are used? Is this data used to adjust the plotter and developer parameters? When was the last time an adjustment to the plotter or developer was needed?

Incoming Material Inspection and Storage:

- a. Is incoming inspection of laminate materials performed? If so, is this 100% or audit inspection? What visual inspection criteria is used? What other testing is done for incoming laminate materials?
- b. Is a purchasing specification in place with the laminate material supplier to control scaled flow, gel time, etc.?
- c. Is the laminate supplier required to submit notification when their raw material suppliers or parameters (i.e.glass cloth supplier, glass finish type, minor resin changes, manufacturing site, etc.) are changed?

Inner Layer Imaging:

- a. Is inner-layer imaging done in a clean room environment? What class?
- b. Is inner-layer imaging done in a temperature and humidity controlled room? If so, is temperature humidity control tracked by chart recorder? If so, does the chart recorder sound off an alarm for out of control conditions? Is the chart paper regularly checked and changed?
- c. Is dry film or liquid photoimageable resist used? What thickness is used?
- d. How many "shots" are allowed before the artwork is re-inspected and/or re-plotted?
- f Do the exposers use collimated light?
- g. Is post etch punch used to control registration? If not, what other method is used to control registration of the artwork to the innerlayer?
- h. What controls are in place to assure problems with resist wrinkles, adhesion, etc. are caught promptly and corrected?
- i. Is break-point testing used to control developer speed?
- j. Is a feed & bleed system based upon PH or another system in place to control developer solution strength?
- k. Is a first article panel run through the entire circuitization and AOI process?

Inner Layer Etching Process:

- a. Is a first article process used to adjust the etch parameters in order to maintain proper control of trace width?
- b. Are there any special procedures in place to maintain proper control of trace widths for impedance controlled cards?

- c. What type and brand of trace width measuring equipment is in place for measuring trace widths immediately upon exit of the parts from the etching equipment?
- d. Are trace widths measured at the bottom of the trace?
- e. Are trace widths tracked with SPC charts and, if so, how is this data used to control and/or improve the etching process?
- f. Is cupric or amoniactal etching used?
- g. What chemical controls in place to assure consistent etching?

Inner layer AOI:

- a. What type and brand of innerlayer AOI system is in use?
- b. What is the resolution capability of the AOI system?
- c. Is reflective or fluorensence based AOI inspection in use?
- d. Are verification stations in use?
- e. Is a knife repair process used to cut out shorts?
- f. % utilization of AOI and verification station equipment?

Treatment of Inner Layers for Lamination:

- a. What type of inner layer treatment is in use (brown/black oxide, oxide alternative, double treat copper cores, etc.)?
- b. Is vertical dip tank or conveyorized process equipment in use?
- c. How is chemistry replenished and compositions controlled?

Lamination:

- a. If lay-up area is considered to be a clean-room environment, what class is it?
- b. Is pre-preg stored and used on a FIFO basis?
- c. At what age is pre-preg re-tested for scaled flow and gel time?
- d. Is pin lamination or riveting in use for layup?
- e. Are planishing plates used between panels in the layup process?
- f. Are lamination presses vacuum assisted?
- g. Is a separate cool down chamber used?
- h. If the press loses vacuum in the middle of a press cycle will an audible alarm sound?
- i. Are temperature and pressure recorded and verified to be within the specified range for each and every press cycle?
- j. What controls are in place to assure that the stack-up meets the minimum time at temperature requirements for the laminate material being pressed?
- m. Is a first article process used to verify that new stack-ups will press out to the predicted layer thicknesses and overall panel thickness?

Registration:

- a. What brand and model of tooling hole drilling equipment is in use? Is it manual or automatic?
- b. If an x-ray based tooling hole drilling system is in use what is the maximum layer-to-layer registration that the system will allow? How does the system respond if the layer-to-layer registration is greater than the maximum allowed?
- c. If the tooling hole drilling system is not x-ray based, describe how tooling hole drilling accuracy is maintained. Describe how the tooling hole drilling system is used in conjunction with other equipment in order to maintain layer-to-layer registration? Are drilling offsets used?
- d. Are there any post-drilling registration measurement systems in place (i.e. Perfectest, etc.)?
- e. How is registration data fed-back to front end engineering to improve their modeling?
- f. Is there a certain registration threshold at which artwork magnification factors are adjusted and new artwork re-plotted? If so, is this threshold below the customers specification for layer-to-layer registration tolerance?

Drilling:

- a. What quantity of each brand and model of drilling equipment is in use?
- b. What is the maximum stack height, hit count, number of resharpes, panel thickness, and layer count allowed for each of the following drill bit sizes: , 0.010", 0.012", 0.014"

- c. Is post-plating hole roughness measured/monitored and used to make improvements to the drilling operation?
- d. What type of equipment or process is in place to verify that all holes have been drilled completely through?
- e. Is a first article process used to verify that the drilling program is correct and complete?
- f. What is the hole location accuracy capability of the drilling equipment? Is hole location accuracy monitored?

Desmear:

- a. Is a permanganate desmear process primarily used for standard FR4 laminate material? If so, who is the supplier of the permanganate desmear chemistry? Which specific chemistry is used?
- b. Is the permanganate desmear process equipment a conveyORIZED process or a vertical dip tank process?
- c. Is product monitored post-plating to assure adequate plating adhesion to the hole wall through multiple soldering cycles and also to assure the absence of butterfly voids and/or wedge voids?
- d. Is the chemistry composition monitored and controlled to a minimum Cpk of 1.33?
- e. Does the system use automatic replenishment with level control?

PTH and Panel Electrolytic Plating Process:

- a. Identify the brand and model of equipment in use for both the electroless copper and electrolytic copper plating processes. Is the equipment based upon a conveyORIZED or a vertical dip tank design?
- b. Does the equipment use vibration to prevent plating voids in the PTHs?
- c. Who is the supplier of the electroless and electrolytic copper chemistry? Which specific chemistry is used?
- d. Are backlight coupons run on a regular basis to assure adequate electroless copper coverage with no pin holes? How often are the backlight coupons run?
- e. Is the chemistry composition monitored and controlled to a minimum Cpk of 1.33?
- f. How often are electroless copper weight gain coupons run?
- g. Does the system use automatic replenishment with level control?
- h. What is the minimum etch rate to which the micro-etch bath is controlled?
- i. Is the electrolytic copper plating process pattern plating, panel plating, or both or is full-build electroless plating used?
- j. Is reverse pulse, standard dc or both plating processes available? In situations where both processes are available describe what factors are used to determine whether reverse pulse or dc copper plating is used?
- k. Is CVS technology used to control plating bath organics?
- l. Are microsections done for each lot of panels in order to ensure minimum PTH cu plating thickness requirements are met? Is this data tracked and controlled to a Cpk of 1.33?
- m. Is a solder float test done for each lot of panels to monitor for IP Separation? In the event of a failed test, what steps are taken? Is the failed lot immediately scrapped or is further testing done? Is the failed lot the only lot that is scrapped or is further work done to determine the extent of the problem and/or root cause before other "passing" lots in the facility are shipped to customers?

Outer Layer:

- a. Is outer-layer imaging done in a clean room environment? What class?
- b. Is outer-layer imaging done in a temperature and humidity controlled room? If so, is temperature humidity control tracked by chart recorder? If so, does the chart recorder sound off an alarm for out of control conditions?
- c. Is dry film or liquid photoimageable resist used? What thickness is used?
- d. What brand and model of resist laminator and exposure systems are in use? Is the resist laminator a cut-sheet laminator?
- e. Is a step tablet or other method of exposure level control used?
- f. How often are UV lamps changed?
- g. Is laser direct imaging capability available? If so, how is a decision made between use of laser direct imaging and standard UV expose process?
- h. How many "shots" are allowed before the artwork is re-inspected and/or re-plotted?
- i. Do the exposers use collimated light?
- j. What system is used by the expose units to ensure optimal registration/alignment of the artwork to the panel surface?

- k. What controls are in place to assure problems with resist wrinkles, adhesion, etc. are caught promptly and corrected?
- l. Is break-point testing used to control developer speed?
- m. Is a feed & bleed system based upon PH or another system in place to control developer solution strength?
- n. Is a first article panel run through the entire circuitization and AOI process?

Solder Masking Process:

- a. What type of process is used to apply the solder mask (i.e. curtain coat, screening, dry film, etc.)? Identify the brand and model of equipment used to apply the solder mask.
- b. Is a tape test done on each lot in order to assure adequate solder mask adhesion?
- c. How does a solder mask develop operator determine that there is a requirement for no plugged vias?
- d. How is the develop process for "no plugged vias" different from the standard develop process?
- e. Is solder mask imaging done in a clean room environment? What class?
- f. How is solder mask registration controlled?
- g. What is the minimum solder mask web size that is manufacturable when there are requirements for no plugged vias?

Gold Plating (Tab & Selective Gold Plating Process):

- a. Identify the brand and model of equipment used for plating the gold edge tabs. Is this equipment a conveyORIZED edge tab plater or a deep tank gold plating process?
- b. Is the chemistry composition monitored and controlled to a minimum Cpk of 1.33?
- d. Is x-ray fluorescence equipment used to check the nickel and gold plating thickness on each lot? How many measurements are made per lot?
- e. What type of testing is done to monitor plating adhesion?
- f. How often is gold plating porosity testing done?
- g. How often is the hardness and roughness of the gold plated surfaces checked?
- h. Does the plating equipment use automatic replenishment with level control?
- i. Are there any processing operations following gold tab plating which require resist, tape, etc. to be applied to the gold tab surfaces?
- j. Who is the supplier of the gold plating chemistry? Which specific chemistry is used?

Profiling:

- a. Is a first article process used to verify that the router program is correct and that the cards are routed in accordance with the customer outline drawings?
- b. Are router operators aware of the special handling requirements required of gold plated parts? Are gloves required for handling parts with gold edge tabs?
- c. Are brushes for removal of burrs on the panel edges restricted from use on PCBs with gold edge tabs?
- d. What stack height is used for routing? Is tooling adequate to ensure that when there are a large quantity of parts per panel and the panels are routed two or three high that the parts do not move while being routed?
- e. What special processing steps are used to ensure that gold tab commoning bars are not lifted, burred, or twisted during the routing process? Is a multi-pass routing operation used? Are special routing bit designs used for PCBs with gold tab commoning bars?

Organic Solderability Preservative:

- a. Who is the supplier of the OSP? What specific chemistry is used (e.g. Entek 106A(X), Gliccoat E2, Gliccoat F2L, etc.)?
- b. How is the process monitored and controlled to ensure an acceptable OSP thickness?
- c. Is the chemistry composition monitored and controlled to a minimum Cpk of 1.33?
- d. What is the minimum and maximum etch rates to which the micro-etch bath is controlled? How often is a weight loss coupon run to verify the etch rate?
- e. What is the maximum number of passes a PCB is allowed to make through the OSP application process?
- f. What precautions have been taking to ensure that galvanic etch does not occur on PCBs with gold edge tabs?
- g. How often is a solderability test run? Does this test include any T&H, reflow & wash, or other forms of pre-conditioning?

Electrical Testing:

- a. What voltage is isolation testing done at and what is the minimum isolation resistance value?
- b. Is the isolation test method such that each network is tested individually for the total parallel leakage to all other networks in the product as a single measurement? If not, is the electrical tester capable of this method of isolation testing?
- c. What is the maximum resistance value that is used for continuity testing? What is the smallest value that this continuity test threshold value could be set at without creating a large number of false opens?
- d. Are cards marked, stamped, or scribed in a way to signify they have been electrically tested?

Impedance Testing:

- a. What is the brand and model of impedance test equipment in use?
- b. How often is in-house calibration of the impedance test equipment done? Is an air-line used for this calibration?
- c. How often is the equipment sent back to the factory for calibration?
- d. What different impedance test probes are in use (i.e. 50 Ohm, 75 Ohm, 100 Ohm, etc.)?
- e. Is a process in place for differential impedance measurements? If so, what is the configuration of the 4 pin probe?

External Layer AOI Process:

- a. What type and brand of external layer AOI system is in use?
- b. What is the resolution capability of the AOI system?
- c. Is reflective or fluorescence based AOI inspection in use? If it is reflectance based, what techniques are used to keep the copper clean/unoxidized to prevent false rejects? Maximum hold times prior to AOI? Tacky roller use? Clean process used if parts wait too long for AOI?
- d. Are verification stations in use?
- e. Is a knife repair process used to cut out shorts?