Source-sense packages
Evolved packages for next gen HV MOSFETs

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Agenda

- Introduction
- New concept: TO-247 with „source-sense“
  - Impact on efficiency
  - Simulation results
  - Real-world results
- SMD with source-sense
  - Advantages
  - Drawbacks
  - Thermal management concepts
- Summary
- Future work
- Q&A
Introduction – evolution of silicon

- Before SJ: IRFP450 (mid 1990s)
  - Rds(on) = 400mΩ
  - FOM = 32.8 [Ω·nC]

- SJ: SPW47N60C3 (2001)
  - Rds(on) = 70mΩ
  - FOM = 17.6 [Ω·nC]

- SJ: IPW60R045CP (2005)
  - Rds(on) = 45mΩ
  - FOM = 6.75 [Ω·nC]

- Natural progression
  - Rds(on) ∼ 20mΩ
  - FOM ∼ 3.4 [Ω·nC]

→ Faster switching at MUCH higher currents
Introduction – (non)evolution of packaging

- TO-247 package highlights:
  + Thermals
  + $R_{DS(ON)}$
  + Familiar

- $L_S$
- Large
- Thru-Hole

FOM 10x improved, NO package change!
The loss mechanism – Turn-ON

\[ \frac{dI_D}{dt} < \frac{(V_{DRV} - V_{CGS})}{L_S} \]

\[
\begin{align*}
V_{DRV} &= 12 \text{ [V]} \\
V_{CGS} &\approx V_{th} = 3.5 \text{ [V]} \\
L_S &= 2 \text{ [nH]} \\
\end{align*}
\]

\[ \Rightarrow \quad \frac{dI_D}{dt} < 4.25 \left[ \frac{A}{ns} \right] \]
Source-sense concept

■ Overcome

\[ \frac{dI_D}{dt} < \frac{(V_{DRV} - V_{CGS})}{L_S} \]

■ Solution:

Schematic Symbol
Source sense concept

TO-247-4P

ThinPAK 8x8
Turn-ON 25A by 'fast' SJ, 2nH Ls

TO-247-3P Simulation

- Discharging CG
- Turning MOSFET back off!

TO-247-4P Simulation

- No Discharging CG
- MOSFET switches 'normal'

\[ E_{ON} = 67\mu J \]
\[ E_{ON} = 15\mu J \]
Turn-OFF 25A by ‘fast’ SJ, 2nH Ls

TO-247-3P
Simulation

\[ E_{OFF} = 21 \mu J \]

\[ I_D \]

\( C_{OSS} \) carries \( I_D \) after channel is off

\( L_S \) has minimal effect

\[ V_{DRV} \]

\[ V_{LS} \]

TO-247-4P
Simulation

\[ E_{OFF} = 12 \mu J \]

\[ I_D \]

\( C_{OSS} \) carries \( I_D \) after channel is off

\( L_S \) has minimal effect

\[ V_{DRV} \]

\[ V_{LS} \]
Simulation results

Total $E_{SW}$ for

- 3-PIN device: 88uJ
- 4-PIN device: 27uJ
- SAVINGS: 61uJ

Assume 100kHz $f_{SW}$, and 50% time near 25A peak: \(~3W\) savings

Assume 1150W PFC at low-line working \(~97\%\) efficiency: \(~0.25\%\) efficiency increase
Real world measurements

1000W PFC using CoolMOS CP (existing)

Vin = 90V_{AC}

f_{SW} = 100kHz

R_G/Q_G \cong 1/15

Source-sense advantage:

8.0W savings

\sim 0.8\% efficiency gain
Real world measurements

PFC using future silicon concept:

\[
\begin{align*}
\text{Pout} &= 2500\text{W} \\
\text{Vin} &= 230\text{V}_{\text{AC}} \\
\text{f}_{\text{SW}} &= 100\text{kHz} \\
\frac{R_G}{Q_G} &\approx 1/55
\end{align*}
\]

Source-sense advantage:

\[
\begin{align*}
\text{2.5W savings} \\
\sim 0.1\% \text{ efficiency gain}
\end{align*}
\]

\[
\begin{align*}
\text{Pout} &= 1150\text{W} \\
\text{Vin} &= 90\text{V}_{\text{AC}} \\
\text{f}_{\text{SW}} &= 100\text{kHz} \\
\frac{R_G}{Q_G} &\approx 1/55
\end{align*}
\]

Source-sense advantage:

\[
\begin{align*}
\text{2.3W savings} \\
\sim 0.2\% \text{ efficiency gain}
\end{align*}
\]

\[
\begin{align*}
\sim 0.25\% \text{ predicted}
\end{align*}
\]
Excess switching losses eliminated... BUT

Driver reference ‘bouncing’
- CM noise
- EMI
- DM noise
- Requires extra filtering

Fixed $L_S$ still problematic!

$L_S$ adds to $L_{PAR}$
- Loop energy
- Potential avalanche
Source-sense for SMD

Why pick SMD?
+ $L_s$
+ Size
+ Reflow

SMD is the obvious choice...

...so why not?
- $R_{TH(J-HS)}$
- $R_{DS(ON)}$
- Board real estate
SMD – overcoming the last “why nots”

“Absolute lowest $R_{TH(J-HS)}$ is a MUST”

$R_{TH}$ Junction-to-HeatSink

- ThinPAK 8x8
  - J-C
  - C(PCB)
  - PCB-HS
  - J-HS
  - R$_{TH}$ values:
    - ~0.5 K/W
    - ~1.2 K/W
    - ~1.8 K/W
    - ~3.5 K/W

- Large die TO-247
  - J-C
  - C-HS
  - J-HS
  - R$_{TH}$ values:
    - ~0.25 K/W
    - ~1.0 K/W
    - ~1.25 K/W

TO-247 ~2.8X better

Excerpt from AN: “Cooling of ThinPAK 8x8”
SMD – overcoming the last “why nots”

Double sided cooling concept (hypothetical)

ThinPAK 8x8 (Top)
- J-C ~1.0 K/W
- C-HS ~1.8 K/W
- J-HS ~2.8 K/W

ThinPAK 8x8 (Bottom) ~3.5 K/W

ThinPAK 8x8 DSC
- J-HS ~1.6 K/W

(To-247 ~1.25 K/W)

Comparable $R_{TH(J-HS)}$ Feasible
SMD – overcoming the last “why nots”

“R_{DS(ON)} requirement, Board real estate”

ThinPAK 8x8 today:

With FOM law:

“Lowest possible R_{DS(ON)} required”

“Board real estate (vs. vertical)”

Parallel mounting on Mezzanine board

- Achieves same low R_{DS(ON)} as present TO-247
- Versatility and freedom
- Maintains all other advantages
Fixed $L_S$ causes excess switching losses

- “Source-sense” TO-247-4P
  - Eliminates excess switching losses
  - New challenges
    - CM noise
Summary leadless SMD

- "Source-sense" leadless SMD
  - Minimizes CM noise
  - Small → design freedom

- Parallel 2 for low $R_{DS(ON)}$
DSC concept

- Could approach TO-247 thermals
- Keeps other advantages
- Only a concept at present
Future work

- Implement DSC concept
- 25 year warranty for Solar applications
  - Solder joint reliability (over MANY thermal cycles)
- Cavity size $R_{DS(ON)}$
  - New low-voltage package announced:
    - Cavity > TO-220
    - Low $L_S$
    - Smaller than D2PAK
    - DSC possible?

If adapted to HV $\Rightarrow$ Low $R_{DS(ON)}$
Questions?
Thank you for your time

- Anders Lind
Reference: Simulation schematic
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