

SEMICONDUCTOR RESEARCH & DEVELOPMENT CENTER (India)

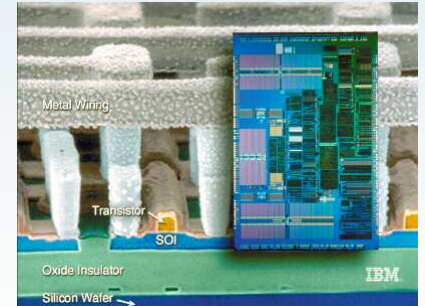


IBM Semiconductor Research and Development Center is Looking for Exceptional Talent for its Enablement Center in Bangalore, India.

"Be a part of an exciting world-wide team developing leading-edge silicon modeling and enablement solutions."

SRDC, Bangalore

The SRDC, Bangalore is the first center outside of US established in 2007 and first of its kind in India. The SRDC group in Bangalore is very active in the areas of PDK Enablement (device modeling, test site design & Design Automation), TCAD & Multiscale modeling (atomistic modeling to predict behaviours of semiconductor devices for IBM's cutting edge technologies), Computational Lithography (OPC/ORC engineering and advanced process modeling focussing on OPC), Process & Device Characterization and Design of IBM's proprietary embedded memory circuits.



Opportunities

Compact Device Modeling & Quality Testing: The selected candidates are responsible for developing compact models for active and passive (both FEOL and BEOL) devices in advanced CMOS, mixed signal, and RF technologies. A related responsibility would be to test the models in the PDK environment before delivering to clients. Doctoral Degree in Electrical Engineering (EE) / Physics with focus on Semiconductor devices preferably FET & Bipolar devices is desired. Master's in EE with strong device focus in thesis can be considered as well for some of the positions.

PDK Design Automation Engineer : Both University freshers and/or experienced professionals in the area of Final kit Testing, DRC & LVS code generation, Pcell & parasitic extraction deck development) who can contribute to IBM's PDK enablement. Masters or PhD's in Elec. Engg from Tier I Universities, or Master's with 3-4 years of relevant industry experience required. Familiarity with Cadence Virtuoso, Assura and Mentor Graphics Calibre tools is required.

Sr. Tech Lead Process Modeling / OPC : Lead a team of OPC modelers for delivering advanced process models for IBM's latest technology nodes. Candidate should have strong knowledge of litho processes, process modeling, and process simulations. Demonstrated ability to interface with lithography engineers, process integration and design teams is important. Candidate must possess a Degree (MS, PhD.) in Computer Science, Electrical Engineering, Physics, or related fields. Experience level can be 7-15 years in relevant field.

Computational Litho Infrastructure: The team develops and supports custom written applications and scripts that support the automation of the Computational Lithography process (prepping the data to be placed on a mask). Our software runs on high performance compute clusters that have thousands of nodes, and span multiple locations. Skills in Perl, Korn Shell, database interaction (db2, mysql), object oriented programming, and web development preferred. Require Master's Degree in Computer Science/Information Technology/Electrical Engg.

Semiconductor Technology characterization and design : This involves three key areas of electrical and defect characterization of state-of-the-art 300mm process technology for sub-32nm nodes. **Device Characterization:** Become an expert at driving device parameters to design specifications. Analyze electrical test data to monitor and drive improvements in device performance and variability. **Defect Characterization:** Monitor, analyze and drive improvements in random and systematic defect densities. Interface with Process and Integration teams to drive yield improvement. **Functional Characterization:** Analyze functional test data from eDRAM / SRAM test chips and suggest improvements to yield, performance and design. Drive Failure Analysis and Diagnostic submissions to determine the root-cause and recommend necessary process changes. Responsibilities include extensive statistical analysis of test data, overall ownership of the test plans including selection of key test structures and setup.

Analog and Memory Design : Strong candidates with background in design and verification of analog and memory test chips. Candidates will have opportunity to work on embedded DRAM, SRAM and 3D memory module development. Desired qualifications are BS/BTech, MS/MTech or PhD degree in Electrical Engineering, Material Science or Physics. Strong background in Semiconductor process and device physics is preferred.

Resumes / CV

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